SSD1815B

Advance Information

LCD Segment / Common Driver with Controller

CMOS

SSD1815B is a single-chip CMOS LCD drivers with controllers for dot-matrix graphic liquid crystal display system. SSD1815B is capable to drive 132 Segments, 64 Commons and 1 icon line by its 197 high voltage driving output.

SSD1815B display data directly from their internal 132 x 65 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from common MCU through 8-bit Parallel or Serial Interface. The selection of whether 6800- or 8080-series compatible Parallel Interface or Serial Peripheral Interface is done by hardware pins configuration.

SSD1815B embeds a DC-DC Converter, an On-Chip Bias Divider and an On-Chip Oscillator which reduce the number of external components. With the advanced design on minimizing power consumption and die/package layout, SSD1815B is suitable for any portable battery-driven applications requiring a long operation period with a compact size.

FEATURES

Dot-matrix Display with separated Icon Line, 132 x 64 + 1 Icon Line
Single Supply Operation, 2.4V ~ 3.5V
Minimum -12.0V LCD Driving Output Voltage
Low Current Sleep Mode
On-Chip Voltage Generator or External LCD Driving Power Supply Selectable
2X / 3X / 4X On-Chip DC-DC Converter
On-Chip Oscillator
Programmable Multiplex ratio in dot-matrix display area, 1Mux ~ 64Mux
On-Chip Bias Divider
Programmable bias ratio, 1/4, 1/5, 1/6, 1/7, 1/8, 1/9
8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface and Serial Peripheral Interface
On-Chip 132 X 65 Graphic Display Data RAM
Re-mapping of Row and Column Drivers
Vertical Scrolling
Display Offset Control
64 Level Internal Contrast Control
External Contrast Control
Programmable LCD Driving Voltage Temperature Coefficients
Available in Gold Bump Die and TAB (Tape Automated Bonding) Package

ORDERING INFORMATION

Table 1 SSD1815B Ordering Information

Ordering Part Number	Seg	Com	Default Bias	Package Form	Reference
SSD1815BZ	132	64 + 1	1/9, 1/7	Gold Bump Die	Figure 2 on page 4
SSD1815BT				70mm Folding TAB	Figure 16 on page 31
SSD1815BT2				48mm Folding TAB	Figure 18 on page 33

BLOCK DIAGRAM

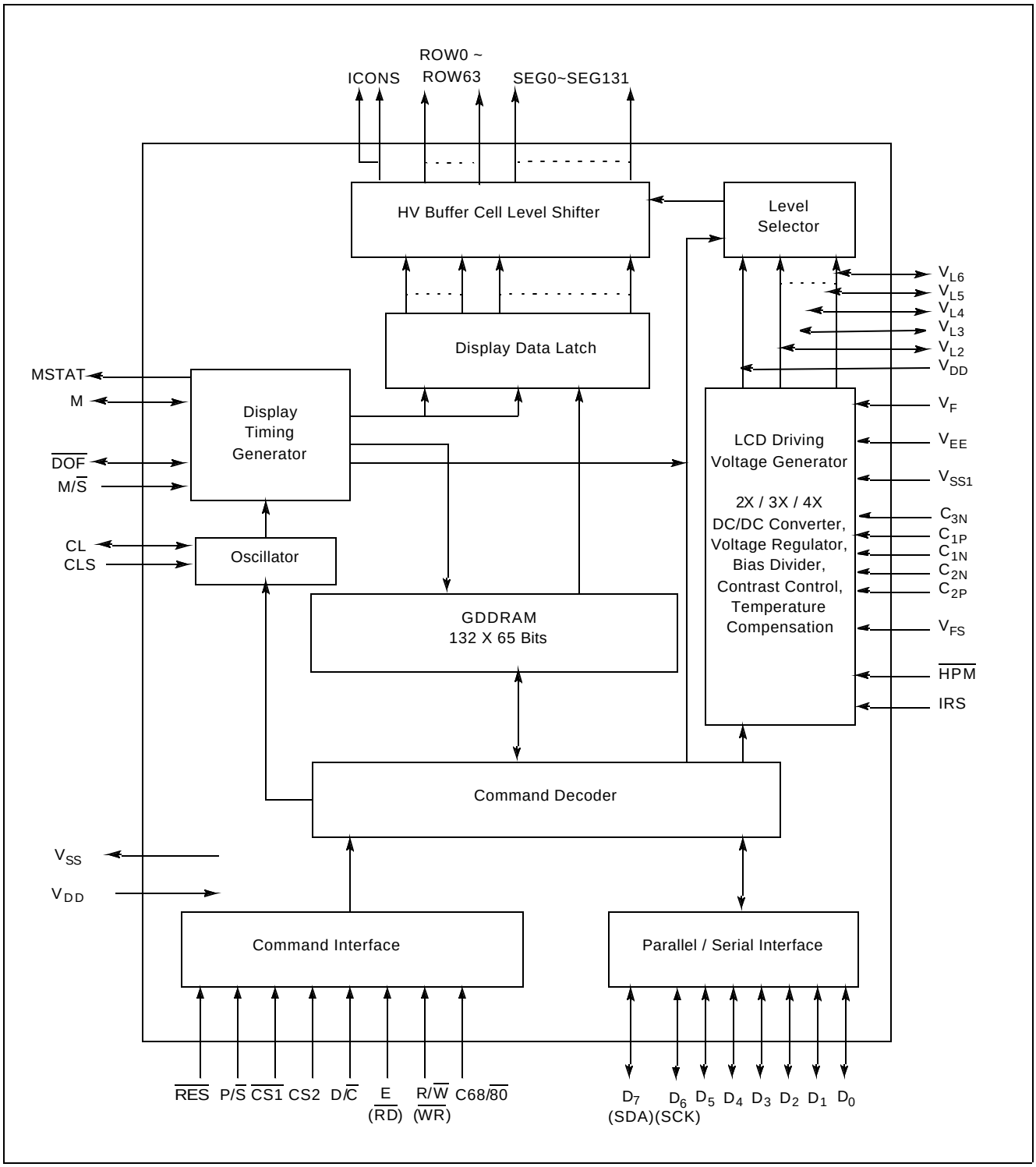
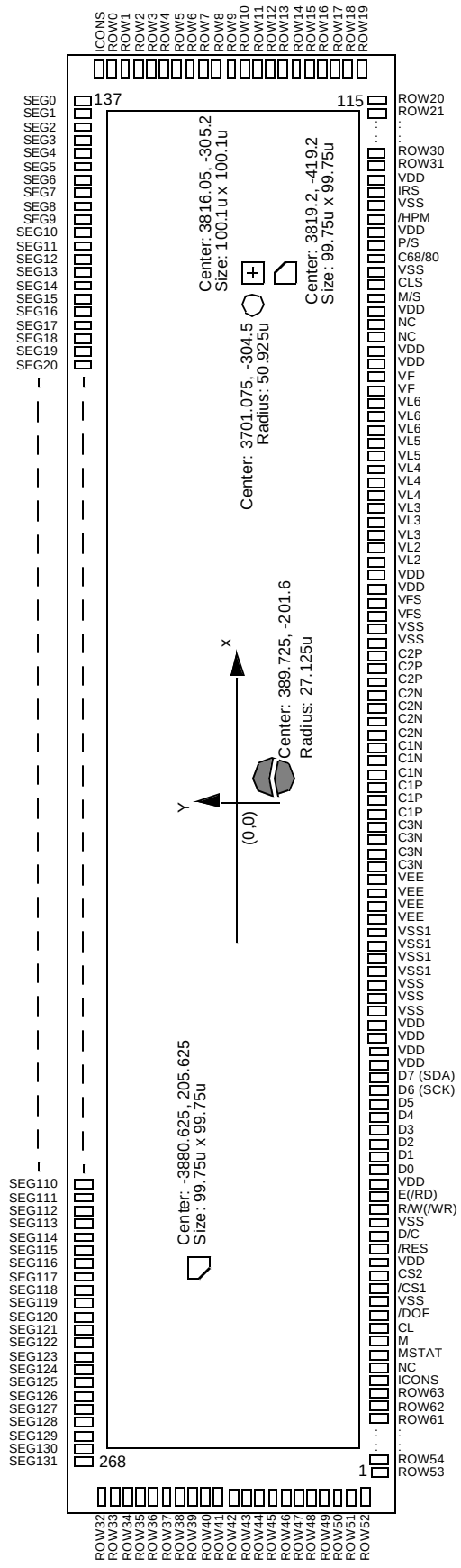


Figure 1 SSD1815B Block Diagram

PIN ARRANGEMENT



Gold Bump Alignment Mark
This alignment mark contains gold bump for IC bumping process alignment and IC identifications. No conductive tracks should be laid underneath this mark to avoid short circuit.

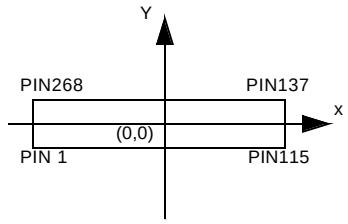
Note:
1. This diagram showing Die Face Up view.
2. Coordinates and Size of all alignment marks are in unit um and w.r.t. center of the chip.

Die Size:	10.977mm X 1.912mm
Die Thickness:	550 +/-25um
Bump Pitch:	76.2 um [Min]
Bump Height:	Nominal 18um
	Tolerance <4um within die
	<8um within lot

Figure 2 SSD1815B Gold Bump Die Pin Assignment

Table 2 SSD1815B Gold Bump Die Pad Coordinates

PAD #	NAME	X	Y	PAD #	NAME	X	Y	PAD #	NAME	X	Y
1	ROW53	-4958.45	-751.98	61	C2N	266.70	-771.93	116	ROW19	5285.18	-768.78
2	ROW54	-4882.15	-751.98	62	C2N	355.60	-771.93	117	ROW18	5285.18	-692.48
3	ROW55	-4805.85	-751.98	63	C2N	444.50	-771.93	118	ROW17	5285.18	-616.18
4	ROW56	-4729.55	-751.98	64	C2N	533.40	-771.93	119	ROW16	5285.18	-539.88
5	ROW57	-4653.25	-751.98	65	C2P	622.30	-771.93	120	ROW15	5285.18	-463.58
6	ROW58	-4576.95	-751.98	66	C2P	711.20	-771.93	121	ROW14	5285.18	-387.28
7	ROW59	-4500.65	-751.98	67	C2P	800.10	-771.93	122	ROW13	5285.18	-310.98
8	ROW60	-4424.35	-751.98	68	VSS	889.00	-771.93	123	ROW12	5285.18	-234.68
9	ROW61	-4348.05	-751.98	69	VSS	977.90	-771.93	124	ROW11	5285.18	-158.38
10	ROW62	-4271.75	-751.98	70	VEE	1066.80	-771.93	125	ROW10	5285.18	-82.08
11	ROW63	-4195.45	-751.98	71	VEE	1155.70	-771.93	126	ROW9	5285.18	-5.78
12	ICONS	-4119.15	-751.98	72	VDD	1244.60	-771.93	127	ROW8	5285.18	70.53
13	NC	-4000.50	-771.93	73	VDD	1333.50	-771.93	128	ROW7	5285.18	146.83
14	MSTAT	-3911.60	-771.93	74	VL2	1422.40	-771.93	129	ROW6	5285.18	223.13
15	M	-3822.70	-771.93	75	VL2	1511.30	-771.93	130	ROW5	5285.18	299.43
16	CL	-3733.80	-771.93	76	VL3	1600.20	-771.93	131	ROW4	5285.18	375.73
17	/DOF	-3644.90	-771.93	77	VL3	1689.10	-771.93	132	ROW3	5285.18	452.03
18	VSS	-3556.00	-771.93	78	VL3	1778.00	-771.93	133	ROW2	5285.18	528.33
19	/CS1	-3467.10	-771.93	79	VL4	1866.90	-771.93	134	ROW1	5285.18	604.63
20	CS2	-3378.20	-771.93	80	VL4	1955.80	-771.93	135	ROW0	5285.18	680.93
21	VDD	-3289.30	-771.93	81	VL4	2044.70	-771.93	136	ICONS	5285.18	757.23
22	/RES	-3200.40	-771.93	82	VL5	2133.60	-771.93				
23	D/C	-3111.50	-771.93	83	VL5	2222.50	-771.93				
24	VSS	-3022.60	-771.93	84	VL6	2311.40	-771.93				
25	R/W	-2933.70	-771.93	85	VL6	2400.30	-771.93				
26	E/RD	-2844.80	-771.93	86	VL6	2489.20	-771.93				
27	VDD	-2755.90	-771.93	87	VE	2578.10	-771.93				
28	D 0	-2667.00	-771.93	88	VE	2667.00	-771.93				
29	D 1	-2578.10	-771.93	89	VDD	2755.90	-771.93				
30	D 2	-2489.20	-771.93	90	VDD	2844.80	-771.93				
31	D 3	-2400.30	-771.93	91	NC	2933.70	-771.93				
32	D 4	-2311.40	-771.93	92	NC	3022.60	-771.93				
33	D 5	-2222.50	-771.93	93	VDD	3111.50	-771.93				
34	D 6	-2133.60	-771.93	94	M/S	3200.40	-771.93				
35	D 7	-2044.70	-771.93	95	CLS	3289.30	-771.93				
36	VDD	-1955.80	-771.93	96	VSS	3378.20	-771.93				
37	VDD	-1866.90	-771.93	97	C68/80	3467.10	-771.93				
38	VDD	-1778.00	-771.93	98	P/S	3556.00	-771.93				
39	VDD	-1689.10	-771.93	99	VDD	3644.90	-771.93				
40	VSS	-1600.20	-771.93	100	/HPM	3733.80	-771.93				
41	VSS	-1511.30	-771.93	101	VSS	3822.70	-771.93				
42	VSS	-1422.40	-771.93	102	IRS	3911.60	-771.93				
43	VSS1	-1333.50	-771.93	103	VDD	4000.50	-771.93				
44	VSS1	-1244.60	-771.93	104	ROW31	4119.15	-751.98				
45	VSS1	-1155.70	-771.93	105	ROW30	4195.45	-751.98				
46	VSS1	-1066.80	-771.93	106	ROW29	4271.75	-751.98				
47	VEE	-977.90	-771.93	107	ROW28	4348.05	-751.98				
48	VEE	-889.00	-771.93	108	ROW27	4424.35	-751.98				
49	VEE	-800.10	-771.93	109	ROW26	4500.65	-751.98				
50	VEE	-711.20	-771.93	110	ROW25	4576.95	-751.98				
51	C3N	-622.30	-771.93	111	ROW24	4653.25	-751.98				
52	C3N	-533.40	-771.93	112	ROW23	4729.55	-751.98				
53	C3N	-444.50	-771.93	113	ROW22	4805.85	-751.98				
54	C3N	-355.60	-771.93	114	ROW21	4882.15	-751.98				
55	C1P	-266.70	-771.93	115	ROW20	4958.45	-751.98				
56	C1P	-177.80	-771.93								
57	C1P	-88.90	-771.93								
58	C1N	0.00	-771.93								
59	C1N	88.90	-771.93								
60	C1N	177.80	-771.93								



Die Size: 10.977mm X 1.912mm
Bump Height:
- nominal: 18um
- tolerance:<4um (within die)
<6um (within wafer)
<8um (within lot)

Unit in um unless otherwise specified.

Die Size: 10.977mm X 1.912mm
Bump Size:

Pad #	X [um]	Y [um]	Pad #	X [um]	Y [um]	Pad #	X [um]	Y [um]	Pad #	X [um]	Y [um]
1 - 12	43.5	101.6	116 - 136	101.6	43.5	137 - 268	43.5	101.6	269 - 289	101.6	43.5
13 - 103	61.7	61.7	Gold bump width tolerance: +/- 3um.								
104 - 115	43.5	101.6									

PAD #	NAME	X	Y	PAD #	NAME	X	Y	PAD #	NAME	X	Y
137	SEG0	4997.65	751.98	203	SEG66	-38.15	751.98	269	ROW32	-5285.18	757.23
138	SEG1	4921.35	751.98	204	SEG67	-114.45	751.98	270	ROW33	-5285.18	680.93
139	SEG2	4845.05	751.98	205	SEG68	-190.75	751.98	271	ROW34	-5285.18	604.63
140	SEG3	4768.75	751.98	206	SEG69	-267.05	751.98	272	ROW35	-5285.18	528.33
141	SEG4	4692.45	751.98	207	SEG70	-343.35	751.98	273	ROW36	-5285.18	452.03
142	SEG5	4616.15	751.98	208	SEG71	-419.65	751.98	274	ROW37	-5285.18	375.73
143	SEG6	4539.85	751.98	209	SEG72	-495.95	751.98	275	ROW38	-5285.18	299.43
144	SEG7	4463.55	751.98	210	SEG73	-572.25	751.98	276	ROW39	-5285.18	223.13
145	SEG8	4387.25	751.98	211	SEG74	-648.55	751.98	277	ROW40	-5285.18	146.83
146	SEG9	4310.95	751.98	212	SEG75	-724.85	751.98	278	ROW41	-5285.18	70.53
147	SEG10	4234.65	751.98	213	SEG76	-801.15	751.98	279	ROW42	-5285.18	-5.78
148	SEG11	4158.35	751.98	214	SEG77	-877.45	751.98	280	ROW43	-5285.18	-82.08
149	SEG12	4082.05	751.98	215	SEG78	-953.75	751.98	281	ROW44	-5285.18	-158.38
150	SEG13	4005.75	751.98	216	SEG79	-1030.05	751.98	282	ROW45	-5285.18	-234.68
151	SEG14	3929.45	751.98	217	SEG80	-1106.35	751.98	283	ROW46	-5285.18	-310.98
152	SEG15	3853.15	751.98	218	SEG81	-1182.65	751.98	284	ROW47	-5285.18	-387.28
153	SEG16	3776.85	751.98	219	SEG82	-1258.95	751.98	285	ROW48	-5285.18	-463.58
154	SEG17	3700.55	751.98	220	SEG83	-1335.25	751.98	286	ROW49	-5285.18	-539.88
155	SEG18	3624.25	751.98	221	SEG84	-1411.55	751.98	287	ROW50	-5285.18	-616.18
156	SEG19	3547.95	751.98	222	SEG85	-1487.85	751.98	288	ROW51	-5285.18	-692.48
157	SEG20	3471.65	751.98	223	SEG86	-1564.15	751.98	289	ROW52	-5285.18	-768.78
158	SEG21	3395.35	751.98	224	SEG87	-1640.45	751.98				
159	SEG22	3319.05	751.98	225	SEG88	-1716.75	751.98				
160	SEG23	3242.75	751.98	226	SEG89	-1793.05	751.98				
161	SEG24	3166.45	751.98	227	SEG90	-1869.35	751.98				
162	SEG25	3090.15	751.98	228	SEG91	-1945.65	751.98				
163	SEG26	3013.85	751.98	229	SEG92	-2021.95	751.98				
164	SEG27	2937.55	751.98	230	SEG93	-2098.25	751.98				
165	SEG28	2861.25	751.98	231	SEG94	-2174.55	751.98				
166	SEG29	2784.95	751.98	232	SEG95	-2250.85	751.98				
167	SEG30	2708.65	751.98	233	SEG96	-2327.15	751.98				
168	SEG31	2632.35	751.98	234	SEG97	-2403.45	751.98				
169	SEG32	2556.05	751.98	235	SEG98	-2479.75	751.98				
170	SEG33	2479.75	751.98	236	SEG99	-2556.05	751.98				
171	SEG34	2403.45	751.98	237	SEG100	-2632.35	751.98				
172	SEG35	2327.15	751.98	238	SEG101	-2708.65	751.98				
173	SEG36	2250.85	751.98	239	SEG102	-2784.95	751.98				
174	SEG37	2174.55	751.98	240	SEG103	-2861.25	751.98				
175	SEG38	2098.25	751.98	241	SEG104	-2937.55	751.98				
176	SEG39	2021.95	751.98	242	SEG105	-3013.85	751.98				
177	SEG40	1945.65	751.98	243	SEG106	-3090.15	751.98				
178	SEG41	1869.35	751.98	244	SEG107	-3166.45	751.98				
179	SEG42	1793.05	751.98	245	SEG108	-3242.75	751.98				
180	SEG43	1716.75	751.98	246	SEG109	-3319.05	751.98				
181	SEG44	1640.45	751.98	247	SEG110	-3395.35	751.98				
182	SEG45	1564.15	751.98	248	SEG111	-3471.65	751.98				
183	SEG46	1487.85	751.98	249	SEG112	-3547.95	751.98				
184	SEG47	1411.55	751.98	250	SEG113	-3624.25	751.98				
185	SEG48	1335.25	751.98	251	SEG114	-3700.55	751.98				
186	SEG49	1258.95	751.98	252	SEG115	-3776.85	751.98				
187	SEG50	1182.65	751.98	253	SEG116	-3853.15	751.98				
188	SEG51	1106.35	751.98	254	SEG117	-3929.45	751.98				
189	SEG52	1030.05	751.98	255	SEG118	-4005.75	751.98				
190	SEG53	953.75	751.98	256	SEG119	-4082.05	751.98				
191	SEG54	877.45	751.98	257	SEG120	-4158.35	751.98				
192	SEG55	801.15	751.98	258	SEG121	-4234.65	751.98				
193	SEG56	724.85	751.98	259	SEG122	-4310.95	751.98				
194	SEG57	648.55	751.98	260	SEG123	-4387.25	751.98				
195	SEG58	572.25	751.98	261	SEG124	-4463.55	751.98				
196	SEG59	495.95	751.98	262	SEG125	-4539.85	751.98				
197	SEG60	419.65	751.98	263	SEG126	-4616.15	751.98				
198	SEG61	343.35	751.98	264	SEG127	-4692.45	751.98				
199	SEG62	267.05	751.98	265	SEG128	-4768.75	751.98				
200	SEG63	190.75	751.98	266	SEG129	-4845.05	751.98				
201	SEG64	114.45	751.98	267	SEG130	-4921.35	751.98				
202	SEG65	38.15	751.98	268	SEG131	-4997.65	751.98				

PIN DESCRIPTIONS

MSTAT

This pin is the static indicator driving output. It is only active in master operation. The frame signal output pin, M, should be used as the back plane signal for the static indicator.

The duration of overlapping could be programmable. See Extended Command Table for details.

This pin becomes high impedance if the chip is operating in slave mode.

M

This pin is the frame signal input/output. In master mode, the pin supplies frame signal to slave devices while in slave mode, the pin receives frame signal from the master device.

CL

This pin is the display clock input/output. In master mode with internal oscillator enabled (CLS pin pulled high), this pin supplies display clock signal to slave devices.

In slave mode or when internal oscillator is disabled, the pin receives display clock signal from the master device or external clock source.

$\overline{DOF}$

This pin is display blanking control between master and slave devices. In master mode, this pin supplies on/off signal to slave devices. In slave mode, this pin receives on/off signal from the master device.

$\overline{CS1}$, CS2

These pins are the chip select inputs. The chip is enabled for MCU communication only when both $\overline{CS1}$ is pulled low and CS2 is pulled high.

$\overline{RES}$

This pin is reset signal input. Initialization of the chip is started once this pin is pulled low. Minimum pulse width for completing the reset procedure is 5us.

D/$\overline{C}$

This pin is Data/Command control pin. When the pin is pulled high, the data at D_7-D_0 is treated as display data. When the pin is pulled low, the data at D_7-D_0 will be transferred to the command register. Details relationship with other MCU interface signals, please refer to the Timing Characteristics Diagrams.

R/$\overline{W}$($\overline{WR}$)

This pin is MCU interface input. When interfacing to an 6800-series microprocessor, this pin will be used as Read/Write (R/$\overline{W}$) selection input. Read mode will be carried out when this pin is pulled high and write mode when low.

When interfacing to an 8080-microprocessor, this pin will be the Write ($\overline{WR}$) input. Data write operation is initiated when this pin is pulled low when the chip is selected.

E($\overline{RD}$)

This pin is MCU interface input. When interfacing to an 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high when the chip is selected.

When connecting to an 8080-microprocessor, this pin receives the Read ($\overline{RD}$) signal. Data read operation is initiated when this pin is pulled low when the chip is selected.

D_7-D_0

These pins are the 8-bit bi-directional data bus to be connected to the MCU in parallel interface mode. D_7 is the MSB while D_0 is the LSB.

When serial mode is selected, D_7 is the serial data input (SDA) and D_6 is the serial clock input (SCK).

V_{DD}

Chip's Power Supply pin. This is also the reference for the DC-DC Converter output and LCD driving voltages.

V_{SS}

Ground. A reference for the logic pins.

V_{SS1}

Input for internal DC-DC converter. The voltage of generated, V_{EE}, equals to the multiple factor times the potential different between this pin, V_{SS1}, and V_{DD}. The multiple factor, 2X, 3X or 4X, is selected by different connections of the external capacitors. All voltage levels are referenced to V_{DD}.

Note: the potential at this input pin must lower than or equal to V_{SS}.

V_{EE}

This is the most negative voltage supply pin of the chip. It can be supplied externally or generated by the internal DC-DC converter, by turning on the **internal voltage booster** option in the **Set Power Control Register** command.

When using internal DC-DC converter as generator, voltage at this pin is for internal reference only. It CANNOT be used for driving external circuitries.

C_{3N}, C_{1P}, C_{1N}, C_{2N} and C_{2P}

When internal DC-DC voltage converter is used, external capacitor(s) is/are connected between these pins. Different connection will result in different DC-DC converter multiple factor, 2X, 3X or 4X. Detail connections please refer to voltage converter section in the functional block description.

V_{FS}

This is an input pin to provide an external voltage reference for the internal voltage regulator. The function of this pin is only enabled for the External Input chip models which are required special ordering. For normal chip model, please leave this pin **NC (No connection)**.

V_{L2}, V_{L3}, V_{L4} and V_{L5}

These are the LCD driving voltage levels. All these levels are referenced to V_{DD}.

They can be supplied externally or generated by the internal bias divider, by turning on the **output op-amp buffers** option in the **Set Power Control Register** command.

The potential relation of these pins are given as:

$$V_{DD} > V_{L2} > V_{L3} > V_{L4} > V_{L5} > V_{L6}$$

and with bias factor, a,

$$V_{L2} - V_{DD} = 1/a * (V_{L6} - V_{DD})$$
$$V_{L3} - V_{DD} = 2/a * (V_{L6} - V_{DD})$$
$$V_{L4} - V_{DD} = (a-2)/a * (V_{L6} - V_{DD})$$
$$V_{L5} - V_{DD} = (a-1)/a * (V_{L6} - V_{DD})$$

V_{L6}

This pin is the most negative LCD driving voltage. It can be supplied externally or generated by turning on the **internal regulator** option in the **Set Power Control Register** command.

V_F

This pin is the input of the built-in voltage regulator for generating V_{L6}.

When external resistor network is selected (IRS pulled low) to generate the LCD driving level, V_{L6}, two external resistors, R_1 and R_2, should be connected between V_{DD} and V_F, and V_F and V_{L6}, respectively (see application circuit diagrams).

M/$\overline{S}$

This pin is the master/slave mode selection input. When this pin is pulled high, master mode is selected, which CL, M, MSTAT and $\overline{DOF}$ signals will be output for slave devices.

When this pin is pulled low, slave mode is selected, which CL, M, $\overline{DOF}$ are required to be input from master device and MSTAT is high impedance.

CLS

This pin is the internal clock enable pin. When this pin is pulled high, internal clock is enabled.

The internal clock will be disabled when it is pulled low, an external clock source must be input to CL pin for normal operation.

C68/$\overline{80}$

This pin is MCU parallel interface selection input. When the pin is pulled high, 6800 series interface is selected and when the pin is pulled low, 8080 series interface is selected.

If Serial Interface is selected (P/$\overline{S}$ pulled low), the setting of this pin is ignored, but must be connected to a known logic (either high or low).

P/$\overline{S}$

This pin is serial/parallel interface selection input. When this pin is pulled high, parallel interface mode is selected. When it is pulled low, serial interface will be selected.

Note1: For serial mode, D0, D1, D2, D3, D4, D5, R/W/(WR), E/(RD) is recommended to be connected to Vss.

Note2: Read Back operation is only available in parallel mode.

$\overline{HPM}$

This pin is the control input of High Power Current Mode. The function of this pin is only enabled for High Power model which required special ordering.

For normal models, High Power Mode is disabled and the LCD driving characteristics are the same no matter this pin is pulled High or Low.

Note: This pin must be pulled to either High or Low. Leaving this pin floating is prohibited.

IRS

This is the input pin to enable the internal resistors network for the voltage regulator. When this pin is pulled high, the internal feedback resistors of the internal regulator for generating V_{L6} will be enabled.

When it is pulled low, external resistors, R_1 and R_2, should be connected to V_{DD} and V_F, and V_F and V_{L6}, respectively (see application circuit diagrams).

ROW0 - ROW63

These pins provide the Common driving signals to the LCD panel. See Table 3 on page 9 for the COM signal mapping in SSD1815B.

SEG0 - SEG131

These pins provide the LCD segment driving signals. The output voltage level of these pins is V_{DD} during sleep mode and standby mode.

ICONS

There are two ICONS pins (pin12 and 136) on the chip. Both pins output exactly the same signal. The reason for duplicating the pin is to enhance the flexibility of the LCD layout.

NC

These are the No Connection pins. Nothing should be connected to these pins, nor they are connected together. These pins should be left open individually.

Table 3 ROW pin assignments for COM signals for SSD1815B .

Die Pad Name	SSD1815B
ROW0	COM0
ROW1	COM1
ROW2	COM2
ROW3	COM3
ROW4	COM4
ROW5	COM5
ROW6	COM6
ROW7	COM7
ROW8	COM8
ROW9	COM9
ROW10	COM10
ROW11	COM11
ROW12	COM12
ROW13	COM13
ROW14	COM14
ROW15	COM15
ROW16	COM16
ROW17	COM17
ROW18	COM18
ROW19	COM19
ROW20	COM20
ROW21	COM21
ROW22	COM22
ROW23	COM23
ROW24	COM24
ROW25	COM25
ROW26	COM26
ROW27	COM27
ROW28	COM28
ROW29	COM29
ROW30	COM30
ROW31	COM31
ROW32	COM32
ROW33	COM33
ROW34	COM34
ROW35	COM35
ROW36	COM36
ROW37	COM37
ROW38	COM38
ROW39	COM39
ROW40	COM40
ROW41	COM41
ROW42	COM42
ROW43	COM43
ROW44	COM44
ROW45	COM45
ROW46	COM46
ROW47	COM47
ROW48	COM48
ROW49	COM49
ROW50	COM50
ROW51	COM51
ROW52	COM52
ROW53	COM53
ROW54	COM54
ROW55	COM55
ROW56	COM56
ROW57	COM57
ROW58	COM58
ROW59	COM59
ROW60	COM60
ROW61	COM61
ROW62	COM62
ROW63	COM63

FUNCTIONAL BLOCK DESCRIPTIONS

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the D/$\overline{C}$ pin.

If D/$\overline{C}$ pin is high, data is written to Graphic Display Data RAM (GDDRAM). If it low, the input at D_7-D_0 is interpreted as a Command and it will be decoded and be written to the corresponding command register.

MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D_7-D_0), R/$\overline{W}$($\overline{WR}$), D/$\overline{C}$, E($\overline{RD}$), $\overline{CS1}$ and CS2. R/$\overline{W}$($\overline{WR}$) input high indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. R/$\overline{W}$($\overline{WR}$) input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/$\overline{C}$ input. The E($\overline{RD}$) input serves as data latch signal (clock) when high provided that $\overline{CS1}$ and CS2 are low and high respectively. Refer to Figure 11 on page 26 for Parallel Interface Timing Diagram of 6800-series microprocessors.

In order to match the operating frequency of the GDDRAM with that of the MCU, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 3.

MPU Parallel 8080-series interface

The parallel interface consists of 8 bi-directional data pins (D_7-D_0), E($\overline{RD}$), R/$\overline{W}$($\overline{WR}$), D/$\overline{C}$, $\overline{CS1}$ and CS2. E($\overline{RD}$) input serves as data read latch signal (clock) when low provided that $\overline{CS1}$ and CS2 are low and high respectively. Whether it is display data or status register read is controlled by D/$\overline{C}$. R/$\overline{W}$($\overline{WR}$) input serves as data write latch signal(clock) when high provided that $\overline{CS1}$ and CS2 are low and high respectively. Whether it is display data or command register write is controlled by D/$\overline{C}$. Refer to Figure 12 on page 27 for Parallel Interface Timing Diagram of 8080-series microprocessor.

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

MPU Serial interface

The serial interface consists of serial clock SCK (D_6), serial data SDA (D_7), D/$\overline{C}$, $\overline{CS1}$ and CS2. SDA is shifted into a 8-bit shift register on every rising edge of SCK in the order of D_7, D_6,... D_0. D/$\overline{C}$ is sampled on every eighth clock to determine whether the data byte in the shift register is written to the Display Data RAM or command register at the same clock. Refer to Figure 13 on Page28 for Serial Interface Timing Diagram.

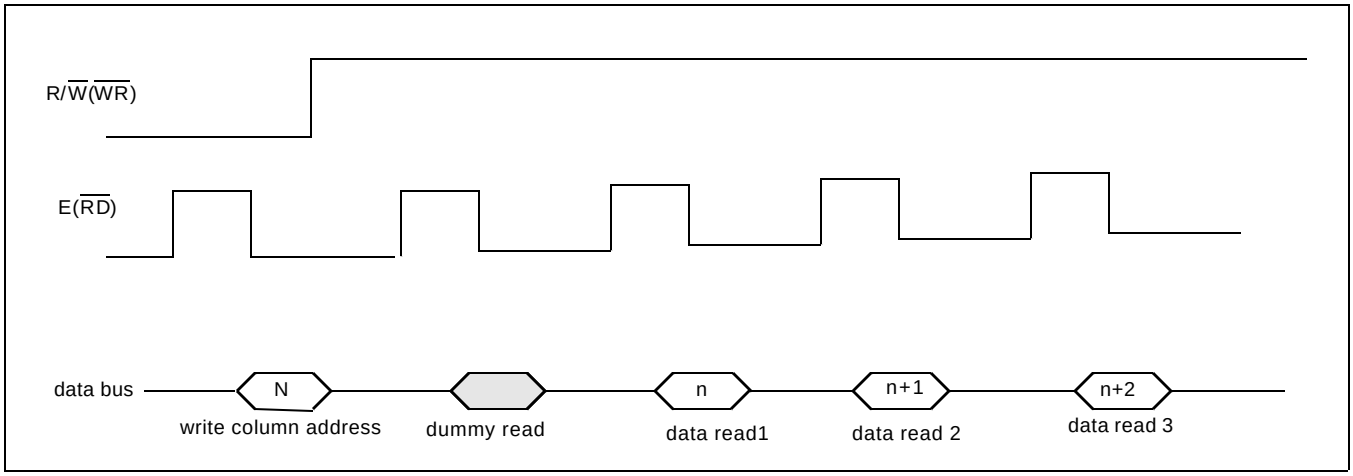


Figure 3 Display Data Read Back Procedure - Insertion of Dummy Read

Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 4). The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

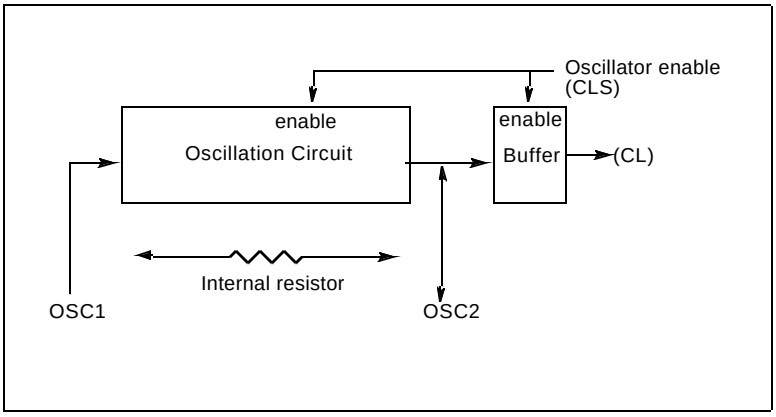


Figure 4 Oscillator Circuitry

LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage required for display driving output. With reference to V_{DD}, it takes a single supply input, V_{SS}, and generate necessary voltage levels. This block consists of:

1. 2X, 3X and 4X DC-DC voltage converter

The built-in DC-DC voltage converter is used to generate the large negative voltage supply with reference to VDD from the voltage input (VSS1). SSD1815B is possible to produce 2X, 3X or 4X boosting from the potential different between V_{SS1} - V_{DD}.

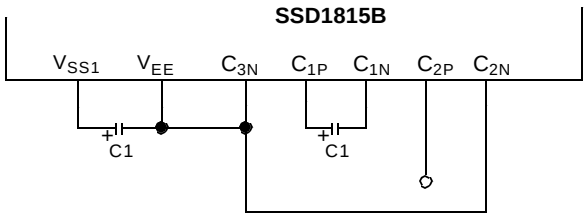
Detail configurations of the DC-DC converter for different boosting multiples are given in Figure 5.

2. Voltage Regulator (Voltages referenced to V_{DD})

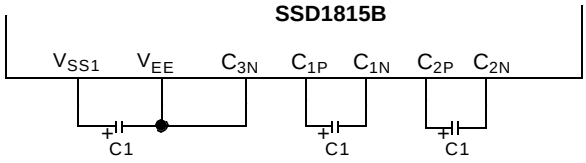
The feedback gain control for LCD driving contrast curves can be selected by IRS pin to either internal (IRS pin = H) or external (IRS pin = L).

If internal resistor network is enabled, eight settings can be selected through software command.

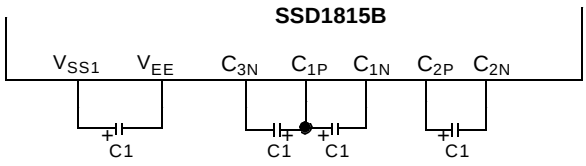
If external control is selected, external resistors are required to be connected between V_{DD} and V_F (R1), and between V_F and V_{L6} (R2). See application circuit diagrams for detail connections.



2X Boosting Configuration



3X Boosting Configuration



4X Boosting Configuration

Remarks:
1. C1 = 0.47 - 1.0uF
2. Boosting input from V_{SS1}.
3. V_{SS1} should be lower potential than or equal to V_{SS}
4. All voltages are referenced to V_{DD}

Figure 5 DC-DC Converter Configurations

3. Contrast Control (Voltages referenced to V_{DD})

Software control of the 64 contrast voltage levels at each voltage regulator feedback gain. The equation of calculating the LCD driving voltage is given as:

$$V_{L6} - V_{DD} = Gain * (1 + \frac{Contrast}{b}) * V_{ref}$$

$$V_{ref} = (\frac{V_{BE} + R * (V_{DD} - V_{SS})}{1 + R})$$

where

Int. Reg. Resistor Ratio Setting	0	1	2	3	4	5	6	7	Ext. Resistor
Gain	-3.37	-3.87	-4.43	-4.99	-5.58	-6.00	-6.67	-7.27	$-(1+R_2/R_1)$
Beta	96.79	96.53	96.33	96.06	95.78	95.54	95.26	95.02	97.62

TC	0 (-0.01%/°C)	2 (-0.15%/°C)	4 (-0.20%/°C)	7 (-0.30%/°C)
VBE	0.02	0.52	0.52	0.51
R	0.73	0.43	0.27	0.12

*Note: There may be a calculation error of max. 6% when comparing with measurement values.

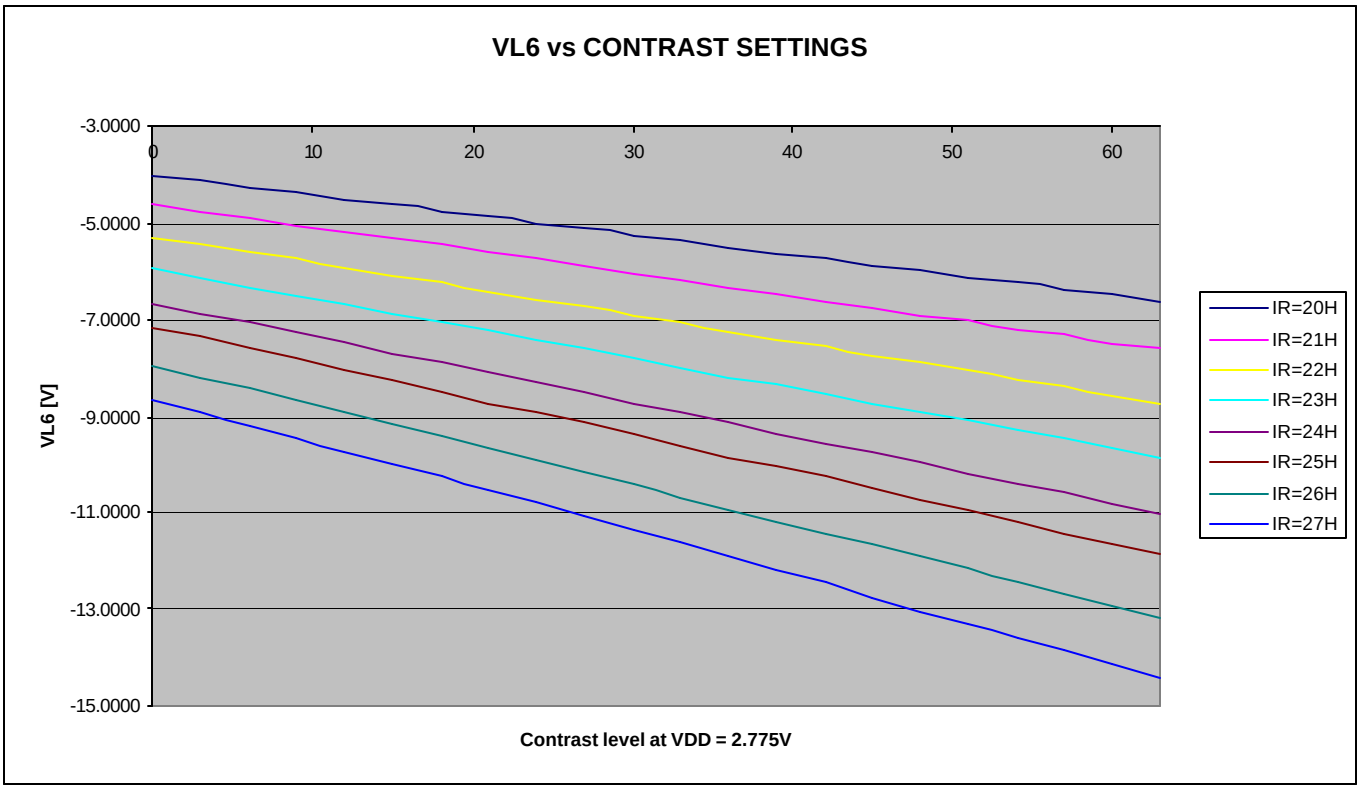


Figure 6 Voltage Regulator Output for Different Gain/Contrast Settings

4. Bias Divider

If the output op-amp buffer option in Set Power Control Register command is enabled, this circuit block will divide the regulator output (V_{L6}) to give the LCD driving levels (V_{L2} - V_{L5}).

A low power consumption circuit design in this bias divider saves most of the display current comparing to traditional design.

Stablizing Capacitors (0.01~0.47uF) are required to be connected between these voltage level pins (V_{L2} - V_{L5}) and V_{DD}. If the LCD panel loading is heavy, four additional resistors are suggested to add to the application circuit as follows:

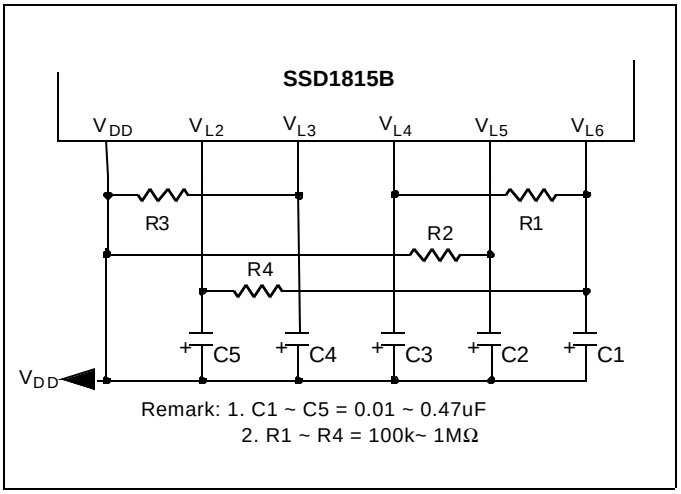


Figure 7 Connections for heavy loading applications

5. Bias Ratio Selection circuitry

SSD1815B can be software selected one of the bias ratios from 1/4, 1/5, 1/6, 1/7, 1/8 and 1/9.

Since there will be slightly different in command pattern for different members, please refer to Command Descriptions section of this data sheet.

6. Self adjust temperature compensation circuitry

This block provides 4 different compensation settings to satisfy various liquid crystal temperature grades by software control. Default temperature coefficient (TC) setting is TC0.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132 x 65 = 8580 bits. Figure 8 on page 14 is a description of the GDDRAM address map.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display. Figure 8 on page 14 shows the case in which the display start line register is set to 38h.

For those GDDRAM out of the display common range, they could still be accessed, for either preparation of vertical scrolling data or even for the system usage.

Reset Circuit

This block includes Power On Reset circuitry and the hardware reset pin, RES. Both of these having the same reset function. Once RES receives a negative reset pulse, all internal circuitry will start to initialize. Minimum pulse width for completing the reset sequence is 5us. Status of the chip after reset is given by:

- Display is turned OFF
- Default Display Display Mode, 132 x 64 + 1 Icon Line
- Normal segment and display data column address mapping (Seg0 mapped to Row address 00h)
- Read-modify-write mode is OFF
- Power control register is set to 000b
- Shift register data clear in serial interface
- Bias ratio is set to default, 1/9
- Static indicator is turned OFF
- Display start line is set to GDDRAM column 0
- Column address counter is set to 00h
- Page address is set to 0
- Normal scan direction of the COM outputs
- Contrast control register is set to 20h
- Test mode is turned OFF
- Temperature Coefficient is set to TC0

Note: Please find more explanation in the Applications Note attached at the back of the specification.

Display Data Latch

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the HV Buffer Cell and Level Selector to output the required voltage level.

The numbers of latches are given by: 132 + 65 = 197

HV Buffer Cell (Level Shifter)

HV Buffer Cell work as a level shifter which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

Level Selector

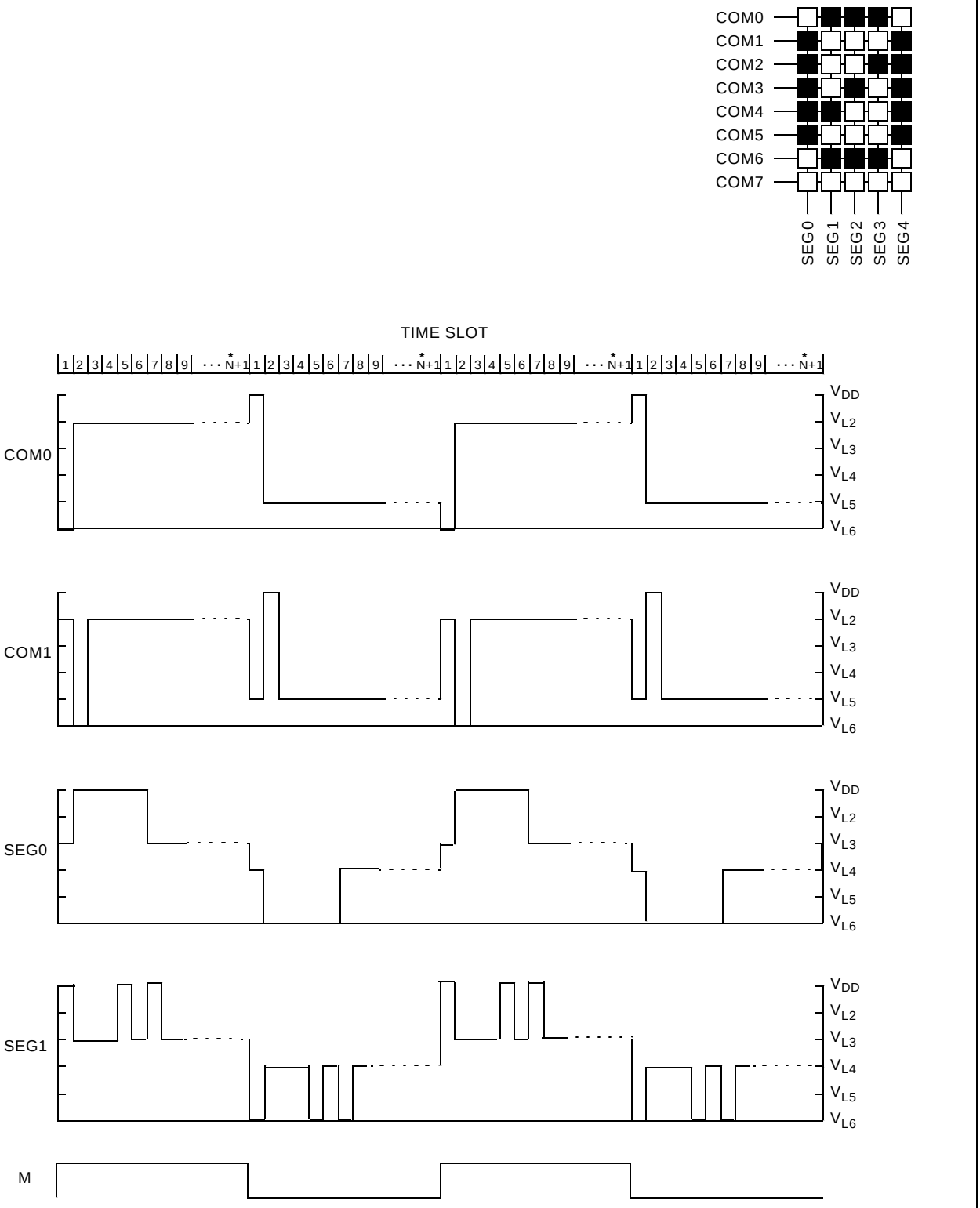
Level Selector is a control of the display synchronization. Display voltage levels can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

LCD Panel Driving Waveform

Figure 9 on page 15 is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveforms provided illustrates the desired multiplex scheme.

RAM Row	RAM Column	Normal	00h	01h	02h	03h	•••••••	80h	81h	82h	83h	Common Pins SSD1815 Normal	Common Pins SSD1815 Remapped
		Remapped	83h	82h	81h	80h	•••••••	03h	02h	01h	00h		
00h	Page 0	D0 (LSB)					•••••••					8	55
01h		D1					•••••••					9	54
02h		D2					•••••••					10	53
03h		D3					•••••••					11	52
04h		D4					•••••••					12	51
05h		D5					•••••••					13	50
06h		D6					•••••••					14	49
07h		D7 (MSB)					•••••••					15	48
08h	Page 1	D0 (LSB)					•••••••					16	47
09h		D1					•••••••					17	46
0Ah		D2					•••••••					18	45
0Bh		D3					•••••••					19	44
0Ch		D4					•••••••					20	43
0Dh		D5					•••••••					21	42
0Eh		D6					•••••••					22	41
0Fh		D7 (MSB)					•••••••					23	40
10h	Page 2	D0 (LSB)					•••••••					24	39
11h		D1					•••••••					25	38
12h		D2					•••••••					26	37
13h		D3					•••••••					27	36
14h		D4					•••••••					28	35
15h		D5					•••••••					29	34
16h		D6					•••••••					30	33
17h		D7 (MSB)					•••••••					31	32
18h	Page 3	D0 (LSB)					•••••••					32	31
19h		D1					•••••••					33	30
1Ah		D2					•••••••					34	29
1Bh		D3					•••••••					35	28
1Ch		D4					•••••••					36	27
1Dh		D5					•••••••					37	26
1Eh		D6					•••••••					38	25
1Fh		D7 (MSB)					•••••••					39	24
20h	Page 4	D0 (LSB)					•••••••					40	23
21h		D1					•••••••					41	22
22h		D2					•••••••					42	21
23h		D3					•••••••					43	20
24h		D4					•••••••					44	19
25h		D5					•••••••					45	18
26h		D6					•••••••					46	17
27h		D7 (MSB)					•••••••					47	16
28h	Page 5	D0 (LSB)					•••••••					48	15
29h		D1					•••••••					49	14
2Ah		D2					•••••••					50	13
2Bh		D3					•••••••					51	12
2Ch		D4					•••••••					52	11
2Dh		D5					•••••••					53	10
2Eh		D6					•••••••					54	9
2Fh		D7 (MSB)					•••••••					55	8
30h	Page 6	D0 (LSB)					•••••••					56	7
31h		D1					•••••••					57	6
32h		D2					•••••••					58	5
33h		D3					•••••••					59	4
34h		D4					•••••••					60	3
35h		D5					•••••••					61	2
36h		D6					•••••••					62	1
37h		D7 (MSB)					•••••••					63	0
38h	Page 7	D0 (LSB)					•••••••					0	63
39h		D1					•••••••					1	62
3Ah		D2					•••••••					2	61
3Bh		D3					•••••••					3	60
3Ch		D4					•••••••					4	59
3Dh		D5					•••••••					5	58
3Eh		D6					•••••••					6	57
3Fh		D7 (MSB)					•••••••					7	56
	Page 8	D0 (LSB)					•••••••					ICONS	ICONS
		Segment Pins	0	1	2	3	•••••••	128	129	130	131		

Figure 8 Graphic Display Data RAM (GDDRAM) Address Map with Display Start Line set to 38h.



* Note : N is the number of multiplex ratio not included Icon.

Figure 9 LCD Driving Waveform for Displaying “0”

COMMAND TABLE

Table 4 Write Command Table (D/$\overline{C}$=0, R/$\overline{W}$($\overline{WR}$)=0, E($\overline{RD}$)=1)

Bit Pattern	Command	Description
$0000X_3X_2X_1X_0$	Set Lower Column Address	Set the lower nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The lower nibble of column address register is reset to 0000b after POR.
$0001X_3X_2X_1X_0$	Set Higher Column Address	Set the higher nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The higher nibble of column address is reset to 0000b after POR.
$00100X_2X_1X_0$	Set Internal Regulator Resistor Ratio	Feedback gain of the internal regulator generating V_{L6} increases as $X_2X_1X_0$ increased from 000b to 111b. After POR, $X_2X_1X_0$ = 100b.
$00101X_2X_1X_0$	Set Power Control Register	X_0=0: turns off the output op-amp buffer (POR) X_0=1: turns on the output op-amp buffer X_1=0: turns off the internal regulator (POR) X_1=1: turns on the internal regulator X_2=0: turns off the internal voltage booster (POR) X_2=1: turns on the internal voltage booster
$01X_5X_4X_3X_2X_1X_0$	Set Display Start Line	Set GDDRAM display start line register from 0-63 using $X_5X_4X_3X_2X_1X_0$. Display start line register is reset to 000000 after POR.
10000001 * * $X_5X_4X_3X_2X_1X_0$	Set Contrast Control Register	Select contrast level from 64 contrast steps. Contrast increases (V_{L6} decreases) as $X_5X_4X_3X_2X_1X_0$ is increased from 000000b to 111111b. $X_5X_4X_3X_2X_1X_0$ = 100000b after POR
$1010000X_0$	Set Segment Re-map	X_0=0: column address 00h is mapped to SEG0 (POR) X_0=1: column address 83h is mapped to SEG0 Refer to Figure 8 on page 14 for example.
$1010001X_0$	Set LCD Bias	X_0=0: POR default bias: 1/9 X_0=1: alternate bias: 1/7 For other bias ratio settings, see “Set 1/4 Bias Ratio” and “Set Bias Ratio” in Extended Command Set.
$1010010X_0$	Set Entire Display On/Off	X_0=0: normal display (POR) X_0=1: entire display on
$1010011X_0$	Set Normal/Reverse Display	X_0=0: normal display (POR) X_0=1: reverse display
$1010111X_0$	Set Display On/Off	X_0=0: turns off LCD panel (POR) X_0=1: turns on LCD panel
$1011X_3X_2X_1X_0$	Set Page Address	Set GDDRAM Page Address (0-8) for read/write using $X_3X_2X_1X_0$
$1100X_3$ * * *	Set COM Output Scan Direction	X_3=0: normal mode (POR) X_3=1: remapped mode, COM0 to COM[N-1] becomes COM[N-1] to COM0 when Multiplex ratio is equal to N. See Figure 8 on page 14 for detail mapping.
11100000	Set Read-Modify-Write Mode	Read-Modify-Write mode will be entered in which the column address will not be increased during display data read. After POR, Read-modify-write mode is turned OFF.
11100010	Software Reset	Initialize internal status registers.
11101110	Set End of Read-Modify-Write Mode	Exit Read-Modify-Write mode. RAM Column address before entering the mode will be restored. After POR, Read-modify-write mode is OFF.

Table 4 Write Command Table (D/$\overline{C}$=0, R/$\overline{W}$($\overline{WR}$)=0, E($\overline{RD}$)=1)

1010110X_0	Set Indicator On/Off	X_0 = 0: indicator off (POR, second command byte is not required) X_0 = 1: indicator on (second command byte required)
* * * * * * X_1X_0	Indicator Display Mode, This second byte command is required ONLY when "Set Indicator On" command is sent.	X_1X_0 = 00: indicator off X_1X_0 = 01: indicator on and blinking at ~1 second interval X_1X_0 = 10: indicator on and blinking at ~1/2 second interval X_1X_0 = 11: indicator on constantly
11100011	NOP	Command result in No Operation
11110000	Test Mode Reset	Reserved for IC testing. Do NOT use.
1111 * * * *	Set Test Mode	Reserved for IC testing. Do NOT use.
* * * * * * * *	Set Power Save Mode (Standby or Sleep)	Standby or sleep mode will be entered using compound commands. Issue compound commands "Set Display Off" followed by "Set Entire Display On".

Table 5 Extended Command Table

Bit Pattern	Command	Description
10101000 00$X_5X_4X_3X_2X_1X_0$	Set Multiplex Ratio	To select multiplex ratio N from 2 to the maximum multiplex ratio (POR value) for each member (including icon line). Max. mux ratio: 65 N = $X_5X_4X_3X_2X_1X_0$ + 2, eg. N = 001111b + 2 = 17
10101001 $X_7X_6X_5X_4X_3X_2X_1X_0$	Set Bias Ratio (X_1X_0) Set TC Value ($X_4X_3X_2$) Modify Osc. Freq. ($X_7X_6X_5$)	X_1X_0 = 00: 1/8 or 1/6; 01: 1/6 or 1/5; 10: 1/9 or 1/7 (POR); 11: Prohibited $X_4X_3X_2$ = 000: -0.01%/ºC (TC0, POR) $X_4X_3X_2$ = 010: -0.15%/ºC (TC2) $X_4X_3X_2$ = 100: -0.20%/ºC (TC4) $X_4X_3X_2$ = 111: -0.30%/ºC (TC7) $X_4X_3X_2$ = 001, 011, 101, 110: Reserved Increase the value of $X_7X_6X_5$ will increase the oscillator frequency and vice versa. Default Mode: $X_7X_6X_5$ = 011 (POR for SSD1815B) : Typ. 19kHz High Frequency Mode: $X_7X_6X_5$ = 110 (For SSD1815B) : Typ. 23kHz
1010101X_0	Set 1/4 Bias Ratio	X_0 = 0: use normal setting (POR) X_0 = 1: fixed at 1/4 bias
11010100 00$X_5X_4$0000	Set Total Frame Phases	The On/Off of the Static Icon is given by 3 phases/1 phase overlapping of the M and MSTAT signals. This command set total phases of the M/MSTAT signals for each frame. The more the total phases, the less the overlapping time and thus the lower the effective driving voltage. X_5X_4 = 00: 3 phases X_5X_4 = 01: 5 phases X_5X_4 = 10: 7 phases (POR) X_5X_4 = 11: 16 phases
11010011 00$X_5X_4X_3X_2X_1X_0$	Set Display Offset	After POR, $X_5X_4X_3X_2X_1X_0$ = 0 After setting mux ratio less than default value, data will be displayed at Center of matrix. To move display towards Row 0 by L, $X_5X_4X_3X_2X_1X_0$ = L To move display away from Row 0 by L, $X_5X_4X_3X_2X_1X_0$ = 64-L Note: max. value of L = (POR default mux ratio - display mux)/2

Table 6 Read Command Table (D/$\overline{C}$=0, R/$\overline{W}$($\overline{WR}$)=1, E=1($\overline{RD}$=0))

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read	D_7=0: indicates the driver is ready for command. D_7=1: indicates the driver is Busy. D_6=0: indicates reverse segment mapping with column address. D_6=1: indicates normal segment mapping with column address. D_5=0: indicates the display is ON. D_5=1: indicates the display is OFF. D_4=0: initialization is completed. D_4=1: initialization process is in progress after $\overline{RES}$ or software reset. $D_3D_2D_1D_0$ = 0010, these 4-bit is fixed to 0010 which could be used to identify as Solomon Systech Device.

Note: Patterns other than that given in Command Table and Extended Command Table are prohibited to enter to the chip as a command. Otherwise, unexpected result will occurs.

Data Read / Write

To read data from the GDDRAM, input High to R/$\overline{W}$($\overline{WR}$) pin and D/$\overline{C}$ pin for 6800-series parallel mode, Low to E($\overline{RD}$) pin and High to D/$\overline{C}$ pin for 8080-series parallel mode. No data read is provided in serial interface mode.

In normal data read mode, GDDRAM column address pointer will be increased by one automatically after each data read. However, no automatic increase will be performed in read-modify-write mode.

Also, a dummy read is required before first valid data is read. See Figure 3 on page 10 in Functional Block Descriptions section for detail waveform diagram.

To write data to the GDDRAM, input Low to R/$\overline{W}$($\overline{WR}$) pin and High to D/$\overline{C}$ pin for both 6800-series and 8080-series parallel mode. For serial interface mode, it is always in write mode. GDDRAM column address pointer will be increased by one automatically after each data write.

It should be noted that, after the automatic column address increment, the pointer will NOT wrap round to 0 when overflow (>131). The incrementation of the pointer stops at 131. Therefore there is a need to re-initialize the pointer when progress to another page address.

Table 7 Automatic Address Increment

D/$\overline{C}$	R/$\overline{W}$($\overline{WR}$)	Action	Auto Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes*1

*1. If read data is issued in read-modify-write mode, address will not be increased automatically.

COMMAND DESCRIPTIONS

Set Lower Column Address

This command specifies the lower nibble of the 8-bit column address of the display data RAM. The column address will be increased by each data access after it is pre-set by the MCU.

Set Higher Column Address

This command specifies the higher nibble of the 8-bit column address of the display data RAM. The column address will be increased by each data access after it is pre-set by the MCU.

Set Internal Regulator Resistors Ratio

This command is to enable any one of the eight internal resistor sets for different regulator gain when using internal regulator resistor network (IRS pin pulled high). In other words, this command is used to select which contrast curve from the eight possible selections. Please refer to Functional Block Descriptions section for detail calculation of the LCD driving voltage.

Set Power Control Register

This command turns on/off the various power circuits associated with the chip. There are three power relating sub-circuits could be turned on/off by this command.

Internal voltage booster is used to generated the large negative voltage supply (V_{EE}) from the voltage input (V_{SS1} - V_{DD}). An external negative power supply is required if this option is turned off.

Internal regulator is used to generate the LCD driving voltage. V_{L6}, from the negative power supply, V_{EE}.

Output op-amp buffer is the internal divider for dividing the different voltage levels (V_{L2}, V_{L3}, V_{L4}, V_{L5}) from the internal regulator output, V_{L6}. External voltage sources should be fed into this driver if this circuit is turned off.

Set Display Start Line

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 63. With value equals to 0, D0 of Page 0 is mapped to COM0. With value equals to 1, D1 of Page0 is mapped to COM0 and so on. Display start line values of 0 to 63 are assigned to Page 0 to 7.

Please refer to Figure 8 on page 14 as an example for display start line set to 56 (38h).

Set Contrast Control Register

This command adjusts the contrast of the LCD panel by changing the LCD drive voltage, V_{L6}, provided by the On-Chip power circuits. V_{L6} is set with 64 steps (6-bit) in the contrast control register by a compound commands.

See Figure 10 for the contrast control flow.

Set Segment Re-map

This command changes the mapping between the display data column addresses and segment drivers. It allows flexibility in mechanical layout of LCD glass design. Please refer to Figure 8 on page 14 for example.

Set LCD Bias

This command is used to select a suitable bias ratio required for driving the particular LCD panel in use.

The selectable values of this command are 1/9 or 1/7.

For other bias ratio settings, extended commands should be used.

Set Entire Display On/Off

This command forces the entire display, including the icon row, to be illuminated regardless of the contents of the GDDRAM. In addition, this command has higher priority than the normal/reverse display.

This command is used together with “Set Display Display ON/OFF” command to form a compound command for entering power save mode. See “Set Power Save Mode” later in this section.

Set Normal/Reverse Display

This command turns the display to be either normal or reversed. In normal display, a RAM data of 1 indicates an illumination on the corresponding pixel, while in reversed display, a RAM data of 0 will turn on the pixel.

It should be noted that the icon line will not affect, that is not be reversed, by this command.

Set Display On/Off

This command is used to turn the display on or off. When display off is issued with entire display is on, power save mode will be entered. See “Set Power Save Mode” later in this section for details.

Set Page Address

This command enters the page address from 0 to 8 to the RAM pager register for read/write operations. Please refer to Figure 8 on page 14 for detail mapping.

Set COM Output Scan Direction

This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly. See Figure 8 on page 14 for the relationship between turning on or off of this feature.

In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will have vertical flipping effect.

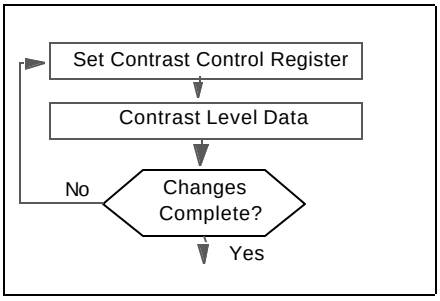


Figure 10 Contrast Control Flow

Set Read-Modify-Write Mode

This command puts the chip in read-modify-write mode in which:

1. column address is saved before entering the mode
2. column address is increased only after display data write but not after display data read.

This Ready-Modify-Write mode is used to save the MCU's loading when a very portion of display area is being updated frequently.

As reading the data will not change the column address, it could be get back from the chip and do some operation in the MCU. Then the updated data could be write back to the GDDRAM with automatic address increment.

After updating the area, "Set End of Read-Modify-Write Mode" is sent to restore the column address and ready for next update sequence.

Software Reset

Issuing this command causes some of the chip's internal status registers to be initialized:

- Read-Modify-Write mode is exited
- Static indicator is turned OFF
- Display start line register is cleared to 0
- Column address counter is cleared to 0
- Page address is cleared to 0
- Normal scan direction of the COM outputs
- Internal regulator resistors Ratio is set to 4
- Contrast control register is set to 20h

Set End of Read-Modify-Write Mode

This command relieves the chip from read-modify-write mode. The column address before entering read-modify-write mode will be restored no matter how much modification during the read-modify-write mode.

Set Indicator On/Off

This command turns on or off the static indicator driven by the M and MSTAT pins.

When the "Set Indicator On" command is sent, the second command byte "Indicator Display Mode" must be followed. However, the "Set Indicator Off" command is a single byte command and no second byte command is required.

The status of static indicator also controls whether standby mode or sleep mode will be entered, after issuing the power save compound command. See "Set Power Save Mode" later in this section.

NOP

A command causing the chip takes No OPeration.

Set Test Mode

This command force the driver chip into its test mode for internal testing of the chip. Under normal operation, users should NOT apply this command.

Set Power Save Mode

Entering Standby or Sleep Mode should be done by using a compound command composed of "Set Display ON/OFF" and "Set Entire Display ON/OFF" commands. When "Set Entire Display ON" is issued when display is OFF, either Standby Mode or Sleep Mode will be entered.

The status of the Static Indicator will determine which power save mode is entered. If static indicator is off, the Sleep Mode will be entered:

- Internal oscillator and LCD power supply circuits are stopped
- Segment and Common drivers output V_{DD} level
- The display data and operation mode before sleep are held
- Internal display RAM can still be accessed

If the static indicator is on, the chip enters Standby Mode which is similar to sleep mode except addition with:

- Internal oscillator is on
- Static drive system is on

Please also be noted that during Standby Mode, if the software reset command is issued, Sleep Mode will be entered. Both power save modes can be exited by the issue of a new software command or by pulling Low at hardware pin $\overline{RES}$.

Status register Read

This command is issued by pulling D/$\overline{C}$ Low during a data read (refer to Figure 11 on page 26 and Figure 12 on page 27 for parallel interface waveforms). It allows the MCU to monitor the internal status of the chip.

No status read is provided for serial mode.

EXTENDED COMMANDS

These commands are used, in addition to basic commands, to trigger the enhanced features designed for the chip.

Set Multiplex Ratio

This command switches default multiplex ratio to any multiplex mode from 2 to the maximum multiplex ratio (POR value), including the icon line. Max. mux ratio: 65

The chip pins ROW0-ROW63 will be switched to corresponding COM signal output, see Table 8 on page 21 for examples of 18 multiplex (including icon line) settings without and with 7 lines display offset for SSD1815B.

It should be noted that after changing the display multiplex ratio, the bias ratio may also need to be adjusted to make display contrast consistent.

Table 8 Row pin assignments for COM signals in 18 mux display (including icon line) with/without 7 line display offset towards ROW0.

Die Pad Name	SSD1815B	
	No Offset	7 lines Offset
ROW0	X	X
ROW1	X	X
ROW2	X	X
ROW3	X	X
ROW4	X	X
ROW5	X	X
ROW6	X	X
ROW7	X	X
ROW8	X	X
ROW9	X	X
ROW10	X	X
ROW11	X	X
ROW12	X	X
ROW13	X	X
ROW14	X	X
ROW15	X	X
ROW16	X	COM0
ROW17	X	COM1
ROW18	X	COM2
ROW19	X	COM3
ROW20	X	COM4
ROW21	X	COM5
ROW22	X	COM6
ROW23	COM0	COM7
ROW24	COM1	COM8
ROW25	COM2	COM9
ROW26	COM3	COM10
ROW27	COM4	COM11
ROW28	COM5	COM12
ROW29	COM6	COM13
ROW30	COM7	COM14
ROW31	COM8	COM15
ROW32	COM9	COM16
ROW33	COM10	X
ROW34	COM11	X
ROW35	COM12	X
ROW36	COM13	X
ROW37	COM14	X
ROW38	COM15	X
ROW39	COM16	X
ROW40	X	X
ROW41	X	X
ROW42	X	X
ROW43	X	X
ROW44	X	X
ROW45	X	X
ROW46	X	X
ROW47	X	X
ROW48	X	X
ROW49	X	X
ROW50	X	X
ROW51	X	X
ROW52	X	X
ROW53	X	X
ROW54	X	X
ROW55	X	X
ROW56	X	X
ROW57	X	X
ROW58	X	X
ROW59	X	X
ROW60	X	X
ROW61	X	X
ROW62	X	X
ROW63	X	X

Note: X - Row pin will output non-selected COM signal.

Set Bias Ratio

Except the 1/4 bias, all other available bias ratios could be selected using this command plus the “Set LCD Bias” command.

For detail setting values and POR default, please refer to the extended command table, Table 5 on page 17.

Set Temperature Coefficient (TC) Value

4 different temperature coefficient settings is selected by this command in order to match various liquid crystal temperature grades. Please refer to the extended command table, Table 5 on page 17, for detail TC values.

Modify Oscillator Frequency

The oscillator frequency can be fine tuned by applying this command. Since the oscillator frequency will be affected by some other factors, this command is not recommended for general usage. Please contact SOLOMON Systech Limited application engineers for more detail explanation on this command.

Set 1/4 Bias Ratio

This command sets the bias ratio directly to 1/4. This bias ratio is especially designed for use in under 12 mux display.

In order to restore to other bias ratio, this command must be executed, with LSB=0, before the “Set Multiplex ratio” or “Set LCD Bias” command is sent.

Set Total Frame Phases

The total number of phases for one display frame is set by this command.

The Static Icon is generated by the overlapping of the M and MSTAT signals. These two pins output either V_{SS} or V_{DD} at same frequency but with phase different.

To turn on the Static Icon, 3 phases overlapping is applied to these signals, while 1 phase overlapping is given to the Off status.

The more the total number of phases in one frame, the less the overlapping time and thus the lower the effective driving voltage at the Static Icon on the LCD panel.

Set Display Offset

This command should be sent ONLY when the multiplex ratio is set less than SSD1815B’s default value.

When a lesser multiplex ratio is set, the display will be mapped in the middle (y-direction) of the LCD, see the no offset columns on Table 8 on page 21. Use this command could move the display vertically within the 64 commons.

To make the Reduced-Mux Com 0 (Com 0 after reducing the multiplex ratio) towards the Row 0 direction for L lines, the 6-bit data in second command should be given by L. An example for 7 line moving towards to Com0 direction is given on Table 8 on page 21.

To move in the other direction by L lines, the 6-bit data should be given by 64-L.

Please note that the display confined within SSD1815B’s default multiplex value. That is the maximum value of L is given by the half of the default value minus the reduced-multiplex ratio. For an odd display mux after reduction, moving away from Row 0 direction will has 1 more step.

MAXIMUM RATINGS

Table 9 Maximum Ratings* (Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{EE}		0 to -12.0	V
V_{in}	Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-30 to +85	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

DC CHARACTERISTICS

Table 10 DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = -30 to 85°C.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	Logic Circuit Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	2.4 1.8	2.7 -	3.5 3.5	V V
I_{AC}	Access Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, Voltage Generator On, 4X DC-DC Converter Enabled, Write accessing, T_{cyc} =3.3MHz, Typ. Osc. Freq., Display On, no panel attached.	-	300	600	µA
I_{DP1}	Display Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, V_{EE} = -8.1V, Voltage Generator Disabled, R/$\overline{W}$($\overline{WR}$) Halt, Typ. Osc. Freq., Display On, V_{L6} - V_{DD} = -9V, no panel attached.	-	60	100	µA
I_{DP2}	Display Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, V_{EE} = -8.1V, Voltage Generator On, 4x DC-DC Converter Enabled, R/$\overline{W}$($\overline{WR}$) Halt, Typ. Osc. Freq., Display On, V_{L6} - V_{DD} = -9V, no panel attached.	-	150	200	µA
I_{SB}	Standby Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, LCD Driving Waveform Off, Typ. Osc. Freq., R/$\overline{W}$($\overline{WR}$) halt.	-	3.5	10	µA
I_{SLEEP}	Sleep Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, LCD Driving Waveform Off, Oscillator Off, R/$\overline{W}$($\overline{WR}$) halt.	-	0.2	5	µA
V_{EE}	LCD Driving Voltage Generator Output (V_{EE} Pin)	Display On, Voltage Generator Enabled, DC-DC Converter Enabled, Typ. Osc. Freq., Regulator Enabled, Divider Enabled.	-12.0	-	-1.8	V
V_{LCD}	LCD Driving Voltage Input (V_{EE} Pin)	Voltage Generator Disabled.	-12.0	-	-1.8	V

Table 10 DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = -30 to 85°C.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH1}	Logic High Output Voltage	I_{out}=-100µA	0.9*V_{DD}	-	V_{DD}	V
V_{OL1}	Logic Low Output Voltage	I_{out}=100µA	0	-	0.1*V_{DD}	V
V_{L6}	LCD Driving Voltage Source (V_{L6} Pin)	Regulator Enabled (V_{L6} voltage depends on Int/Ext Contrast Control)	V_{EE}-0.5	-	V_{DD}	V
V_{L6}	LCD Driving Voltage Source (V_{L6} Pin)	Regulator Disable	-	Floating	-	V
V_{IH1}	Logic High Input voltage		0.8*V_{DD}	-	V_{DD}	V
V_{IL1}	Logic Low Input voltage		0	-	0.2*V_{DD}	V
V_{L2}	LCD Display Voltage Output	Voltage reference to V_{DD}, Bias Divider	-	1/a*V_{L6}	-	V
V_{L3}	(V_{L2}, V_{L3}, V_{L4}, V_{L5}, V_{L6} Pins)	Enabled, 1:a bias ratio	-	2/a*V_{L6}	-	V
V_{L4}			-	(a-2)/a*V_{L6}	-	V
V_{L5}			-	(a-1)/a*V_{L6}	-	V
V_{L6}			-	V_{L6}	-	V
V_{L2}	LCD Display Voltage Input	Voltage reference to V_{DD}, External Voltage Generator, Bias Divider Disabled	V_{L3}	-	V_{DD}	V
V_{L3}	(V_{L2}, V_{L3},V_{L4}, V_{L5}, V_{L6} Pins)		V_{L4}	-	V_{L2}	V
V_{L4}			V_{L5}	-	V_{L3}	V
V_{L5}			V_{L6}	-	V_{L4}	V
V_{L6}			-12V	-	V_{L5}	V
I_{OH}	Logic High Output Current Source	V_{out} = V_{DD}-0.4V	50	-	-	µA
I_{OL}	Logic Low Output Current Drain	V_{out} = 0.4V	-	-	-50	µA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	µA
I_{IL}/I_{IH}	Logic Input Current		-1	-	1	µA
C_{IN}	Logic Pins Input Capacitance		-	5	7.5	pF
ΔV_{L6}	Variation of V_{L6} Output (V_{DD} is fixed)	Regulator Enabled, Internal Contrast Control Enabled, Set Contrast Control Register = 0	-3	0	3	%
	Temperature Coefficient Compensation					
TC0	Flat Temperature Coefficient (POR)	Voltage Regulator Enabled	0	-0.01	-0.12	%/°C
TC2	Temperature Coefficient 2*	Voltage Regulator Enabled	-0.12	-0.15	-0.17	%/°C
TC4	Temperature Coefficient 4*	Voltage Regulator Enabled	-0.17	-0.20	-0.25	%/°C
TC7	Temperature Coefficient 7*	Voltage Regulator Enabled	-0.25	-0.30	-	%/°C

* The formula for the temperature coefficient is:

$$TC(\%) = \frac{V_{ref} \text{ at } 50°C - V_{ref} \text{ at } 0°C}{50°C - 0°C} \times \frac{1}{V_{ref} \text{ at } 25°C} \times 100\%$$

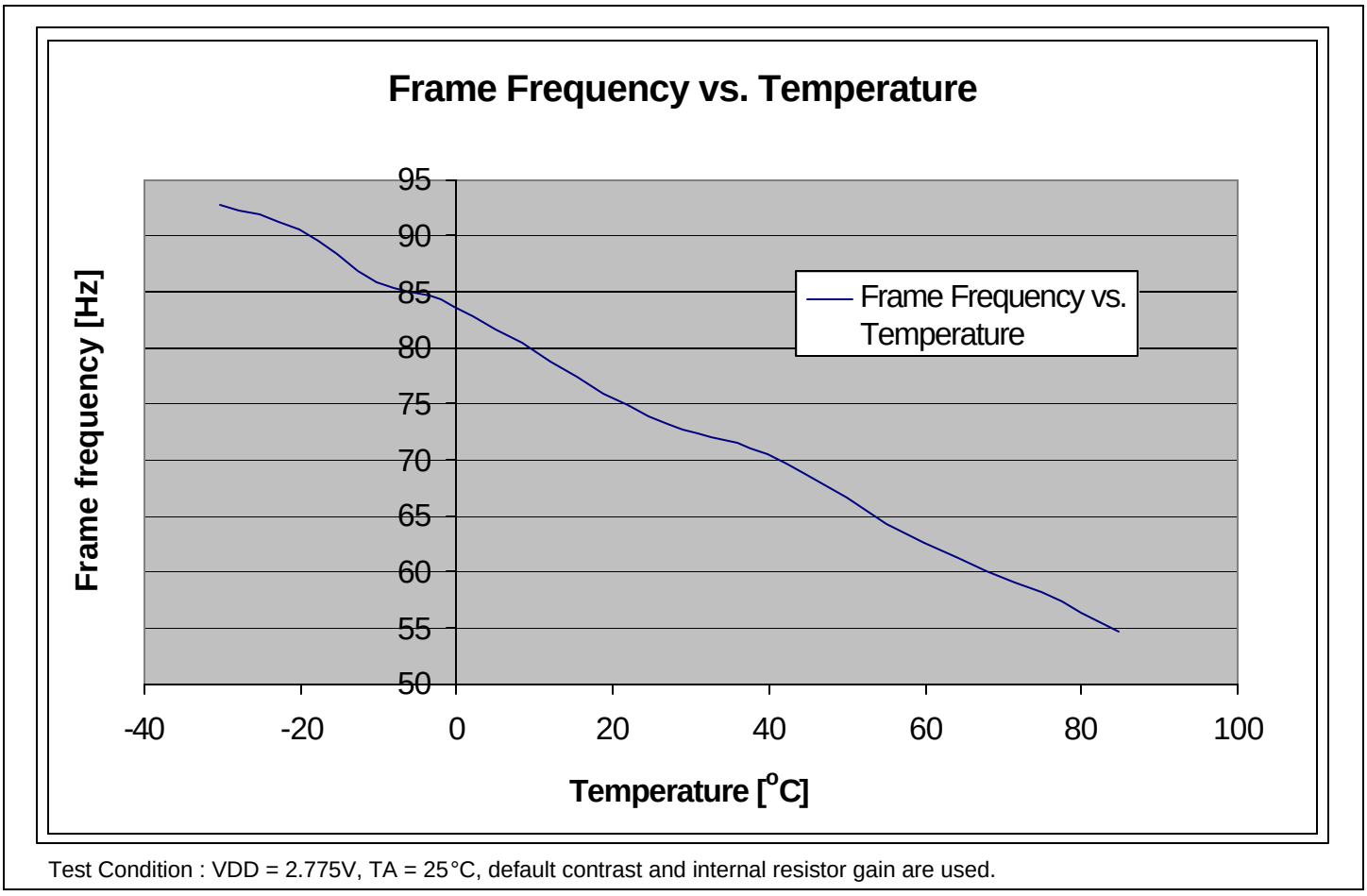
AC CHARACTERISTICS

Table 11 AC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display Timing Generator for: • SSD1815B	Internal Oscillator Enabled (default), V_{DD} = 2.7V Remark: Oscillation Frequency vs Temperature change (-20°C to 70°C): -0.5%/°C *	17	19	21	kHz
F_{FRM}	Frame Frequency for: • SSD1815B	132 x 64 Graphic Display Mode, Display ON, Internal Oscillator Enabled 132 x 64 Graphic Display Mode, Display ON, Internal Oscillator Disabled, External clock with freq., F_{ext}, feeding to CL pin.		$\frac{F_{OSC}}{4 \times 65}$		Hz

* The formula for Oscillation Frequency vs Temperature Change:

$$\%change\ (F_{osc}) = \frac{F_{osc}\ at\ 70°C - F_{osc}\ at\ -20°C}{70°C - (-20°C)} \times \frac{1}{F_{osc}\ at\ 25°C} \times 100\%$$



Test Condition : VDD = 2.775V, TA = 25°C, default contrast and internal resistor gain are used.

Table 12 6800-Series MPU Parallel Interface Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = -30 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	- -	- -	ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

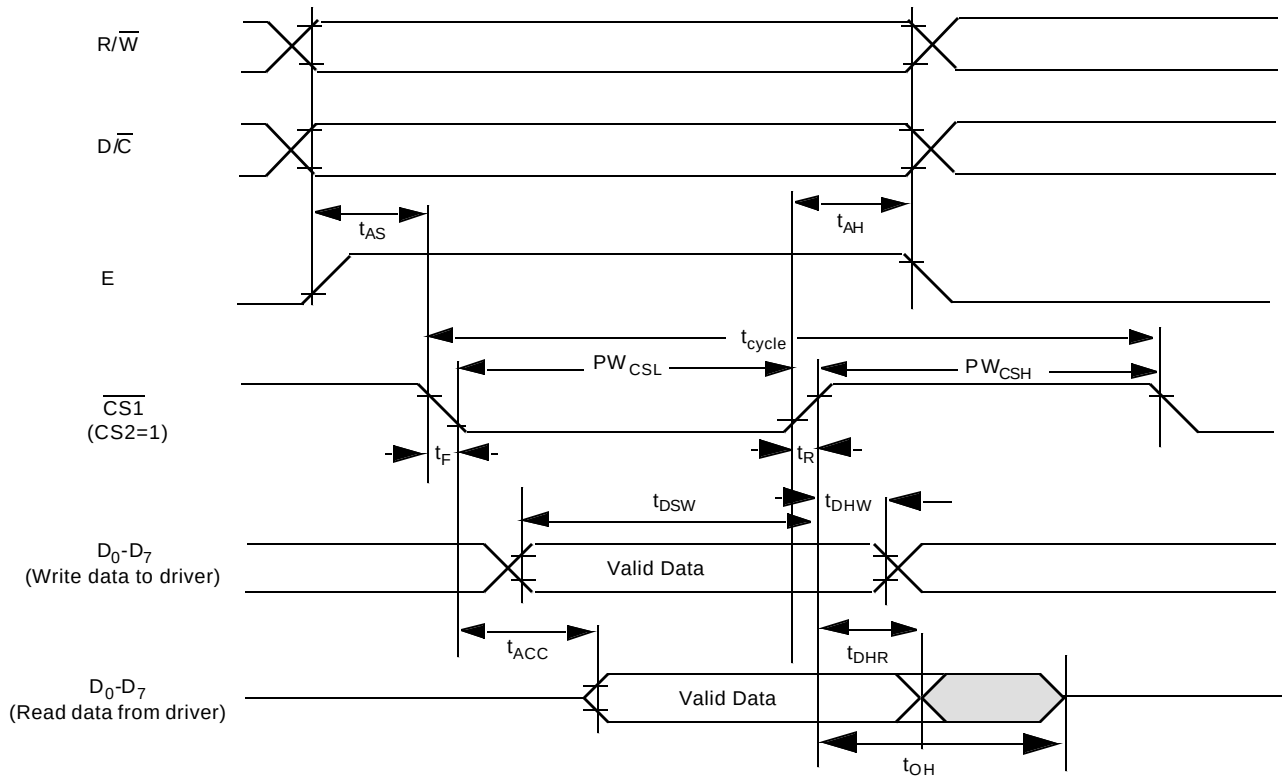


Figure 11 6800-series MPU Parallel Interface Characteristics

Table 13 8080-Series MPU Parallel Interface Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = -30 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	- -	- -	ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

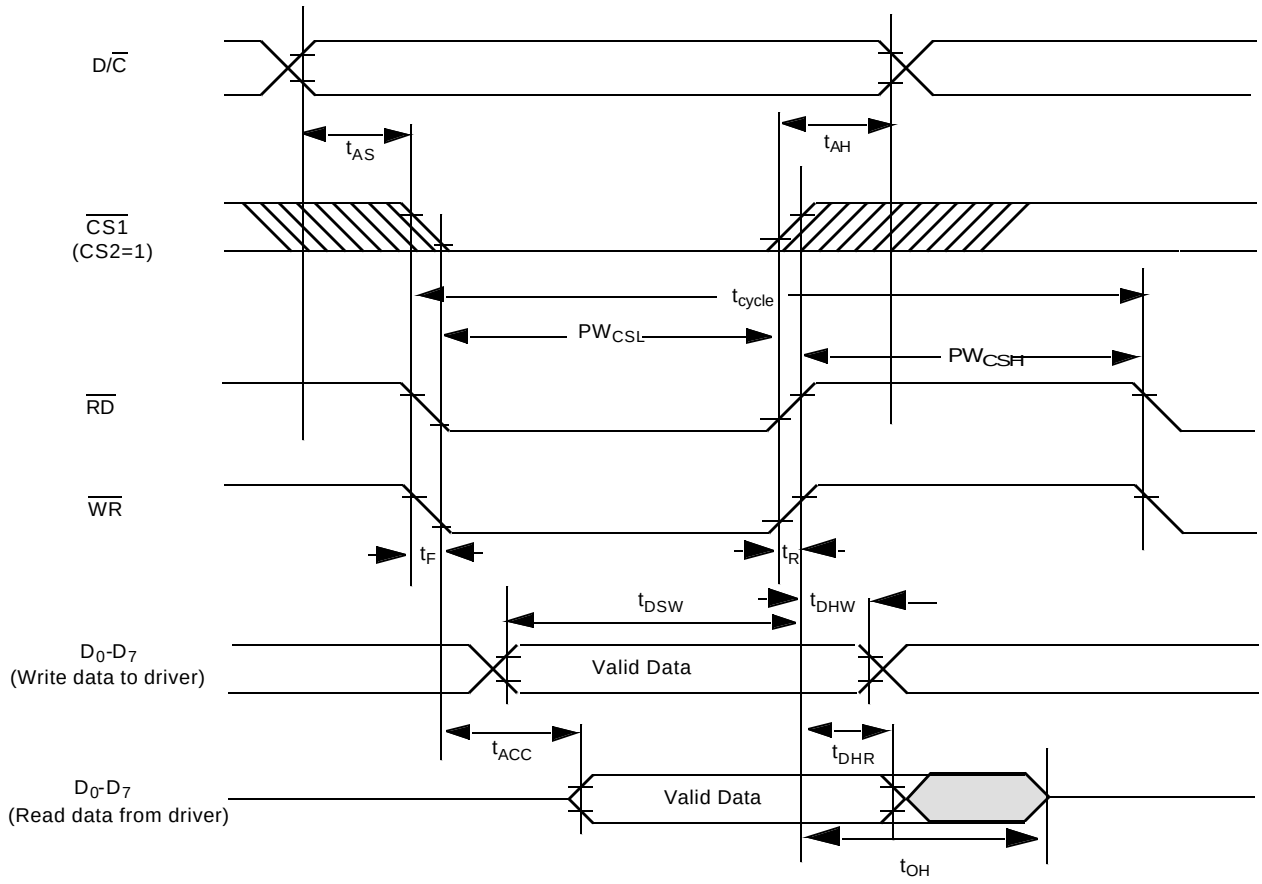


Figure 12 8080-series MPU Parallel Interface Characteristics

Table 14 Serial Interface Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = -30 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time (for D_7 input)	120	-	-	ns
t_{CSH}	Chip Select Hold Time (for D_0 input)	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

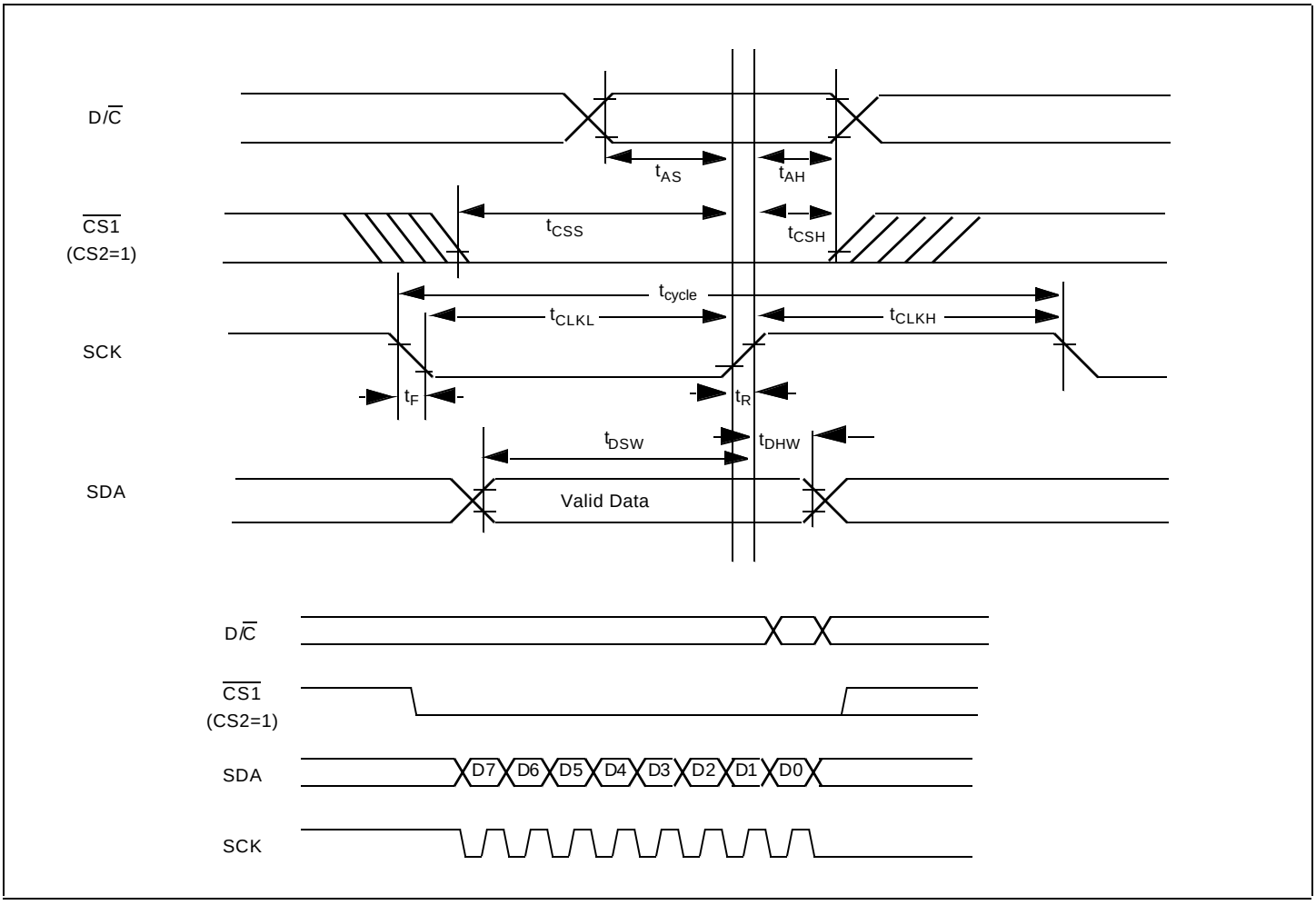
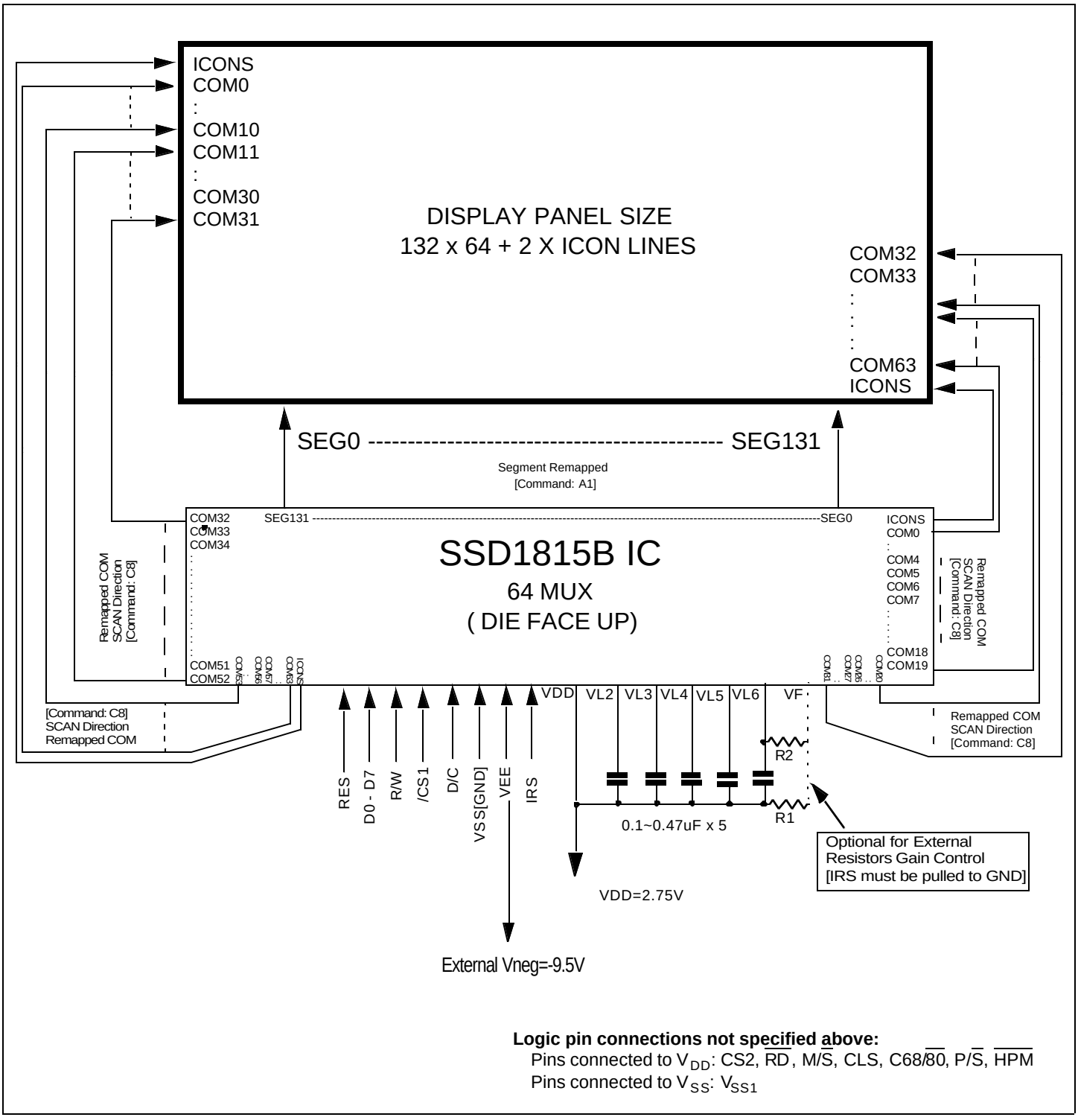


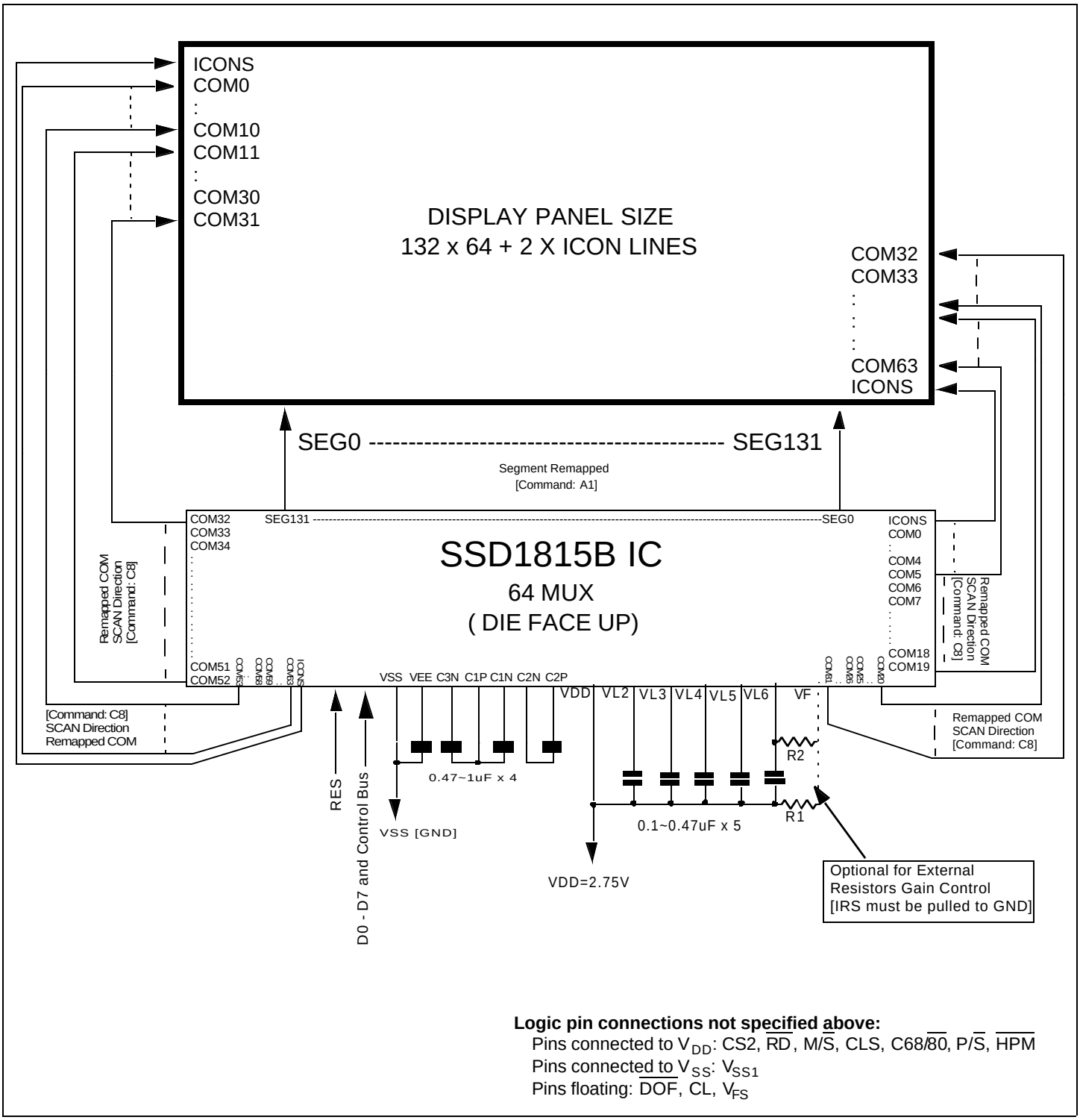
Figure 13 Serial Interface Characteristics

APPLICATION EXAMPLES



Logic pin connections not specified above:
Pins connected to V_{DD}: CS2, $\overline{RD}$, M/$\overline{S}$, CLS, C68/$\overline{80}$, P/$\overline{S}$, $\overline{HPM}$
Pins connected to V_{SS}: V_{SS1}

Figure 14 Application Circuit of 132 x 64 plus 2 icon lines using SSD1815B, configured with: external V_{EE}, internal regulator, divider mode enabled (Command: 2B), 6800-series MPU parallel interface, internal oscillator and master mode.



Logic pin connections not specified above:

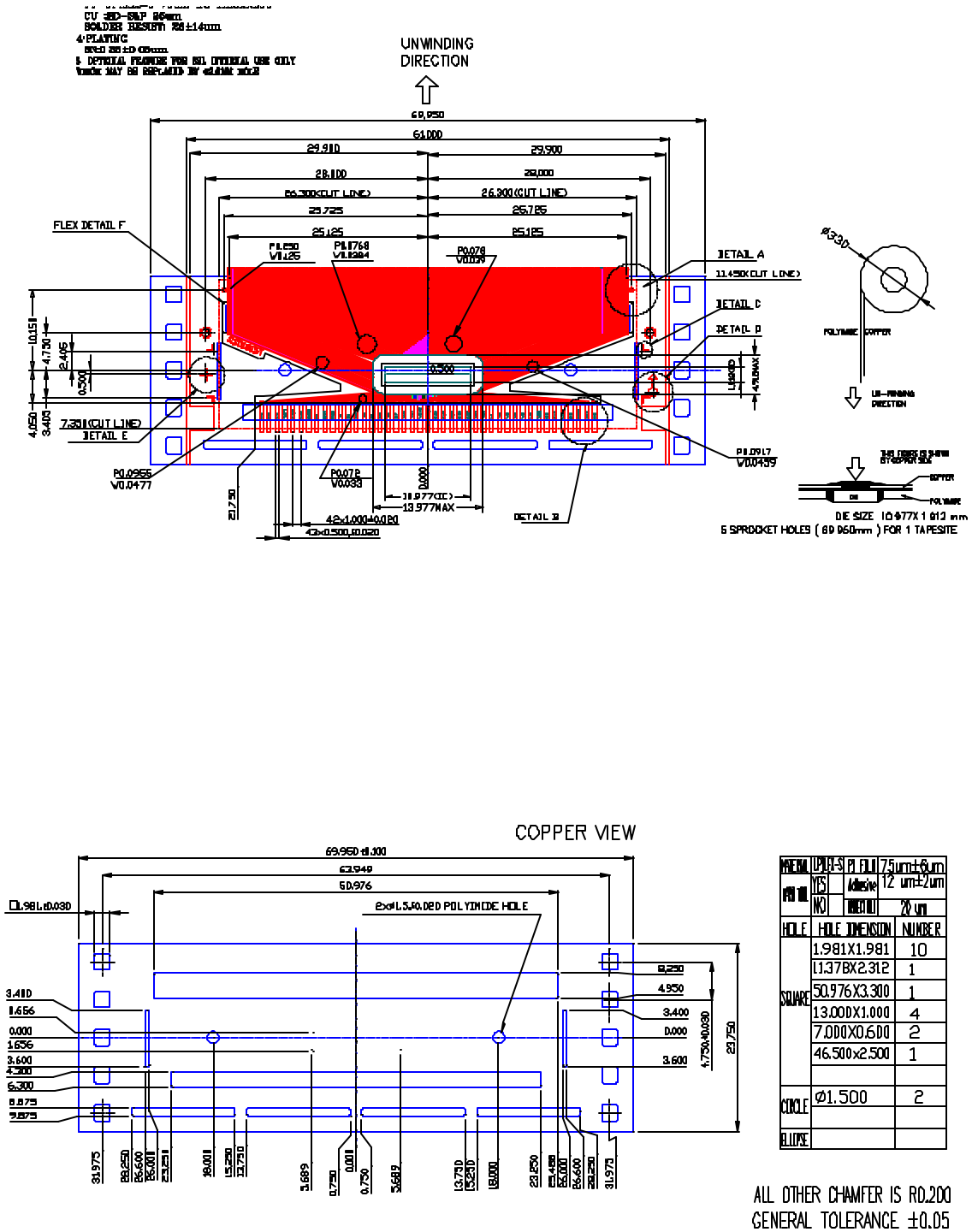
Pins connected to V_{DD}: CS2, $\overline{RD}$, M/$\overline{S}$, CLS, C68/$\overline{80}$, P/$\overline{S}$, $\overline{HPM}$

Pins connected to V_{SS}: V_{SS1}

Pins floating: $\overline{DOF}$, CL, V_{FS}

Figure 15 Application Circuit of 132 x 64 plus 2 icon lines using SSD1815B, configured with all internal power control circuit enabled, 6800-series MPU parallel interface, internal oscillator and master mode.

APPENDIX A - TAB INFORMATION



HOLE	HOLE DIMENSION	NUMBER
SQUARE	1.981X1.981	10
	11.37BX2.312	1
	50.976X3.300	1
	13.000X1.000	4
	7.000X0.600	2
	46.500x2.500	1
CIRCLE	Ø1.500	2
ELLIPSE		

Figure 16 SSD1815BT TAB Drawing 1/2

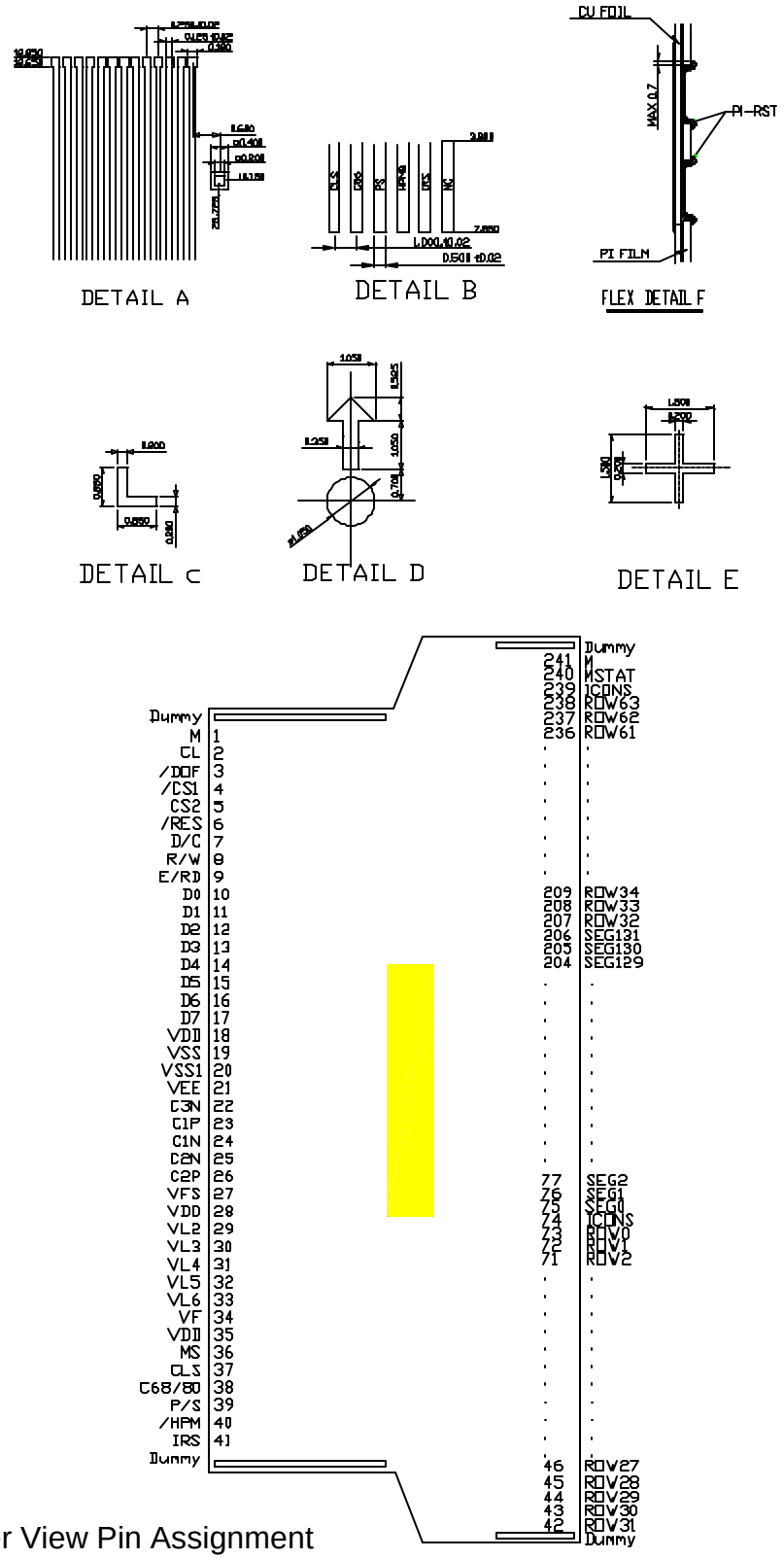


Figure 17 SSD1815BT TAB Drawing 2/2

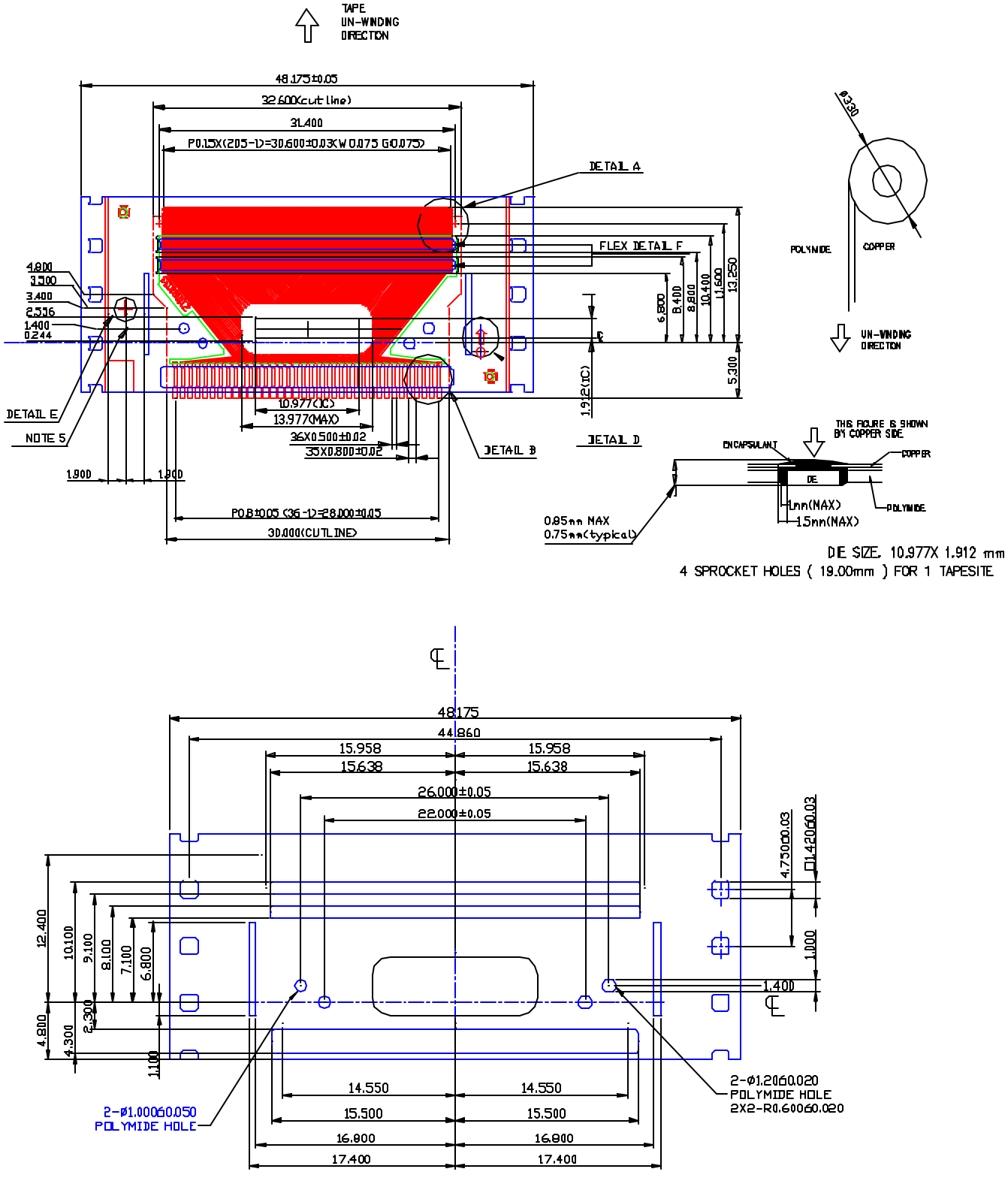
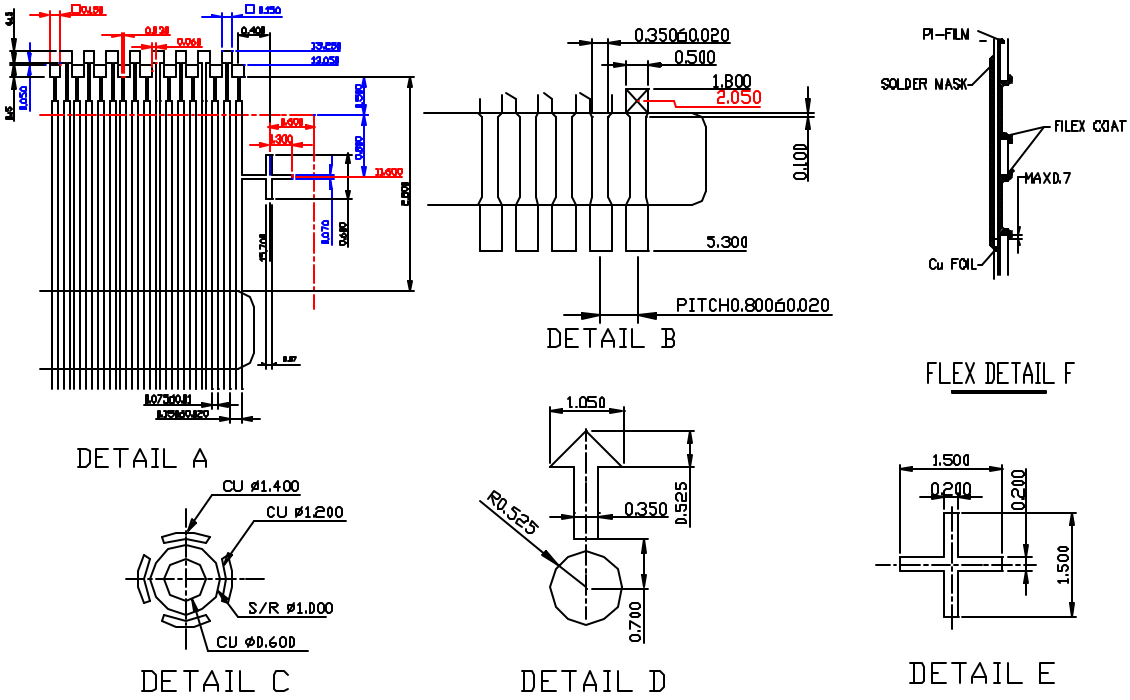
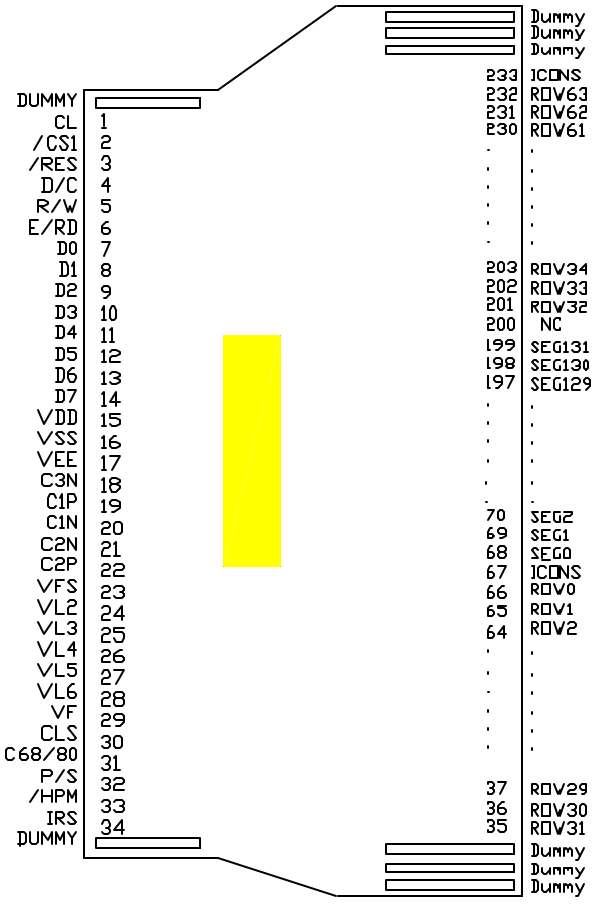


Figure 18 SSD1815BT2 TAB Drawing 1/2

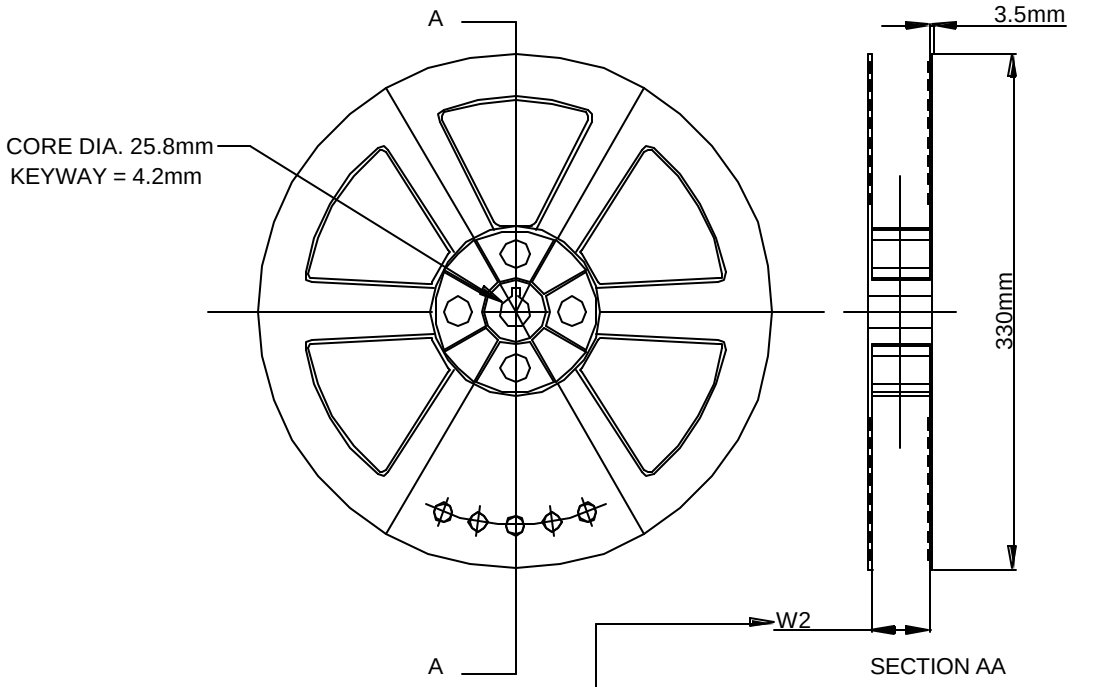




Internal Connections:
V_{DD}: CS2, M/$\overline{S}$
V_{SS}: V_{SS1}

Figure 19 SSD1815BT2 TAB Drawing 2/2

APPENDIX B - TAB WHEEL INFORMATION



MATERIAL: HIGH IMPACT POLYSTYRENE (HIPS)
SURFACE RESISTIVITY: 1 X 10^5 OHM MIN
1 X 10^9 OHM MAX
TAPE LENGTH = 20m

	35mm TAB	48mm TAB	70mm TAB
W2	37±0.2 mm	50±0.2 mm	70±0.2 mm

Figure 20 TAB Wheel Mechanical Drawing